PM 9200302014S1
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BENDER ET AL.

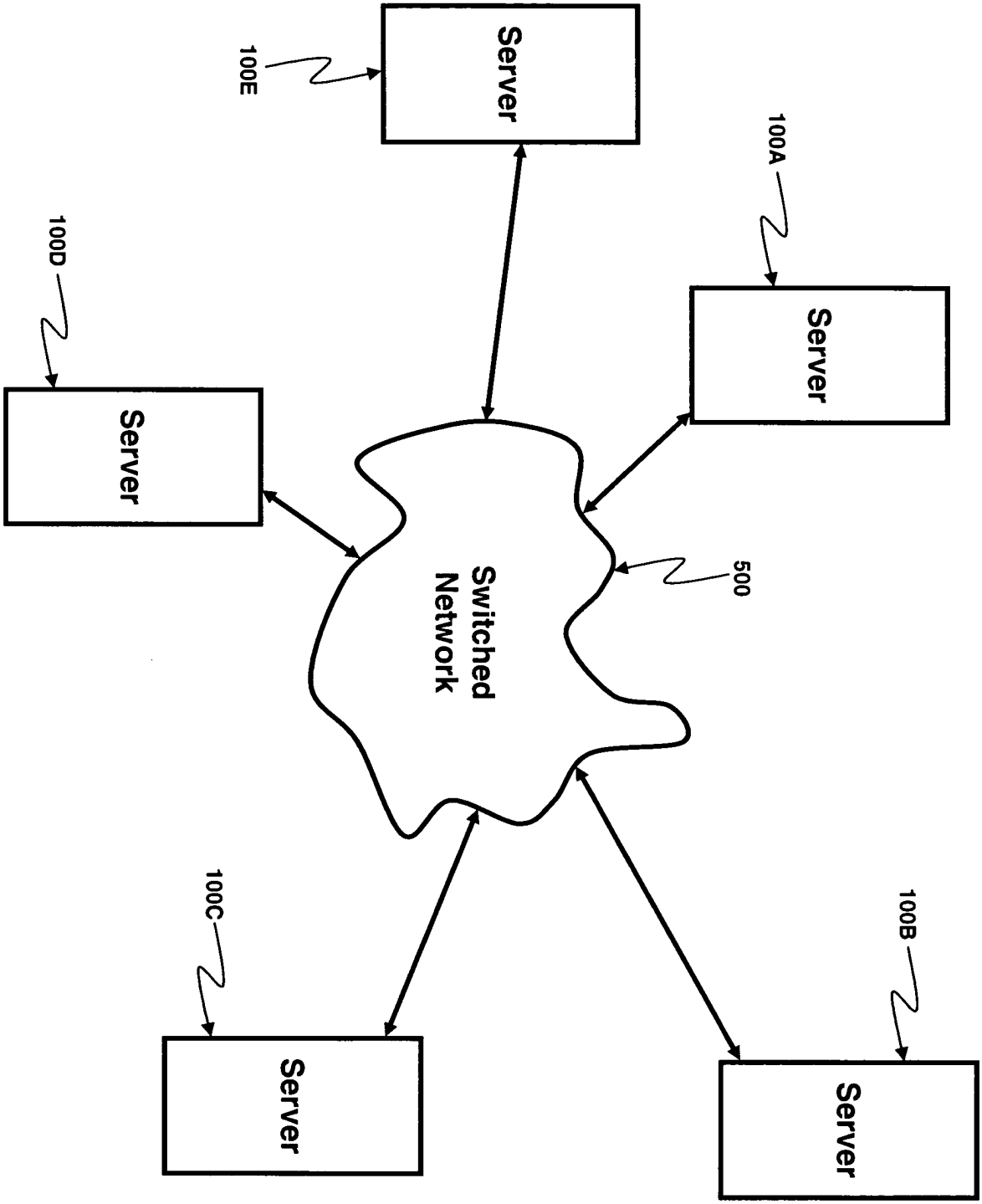

Figure 1

Pon920030201251
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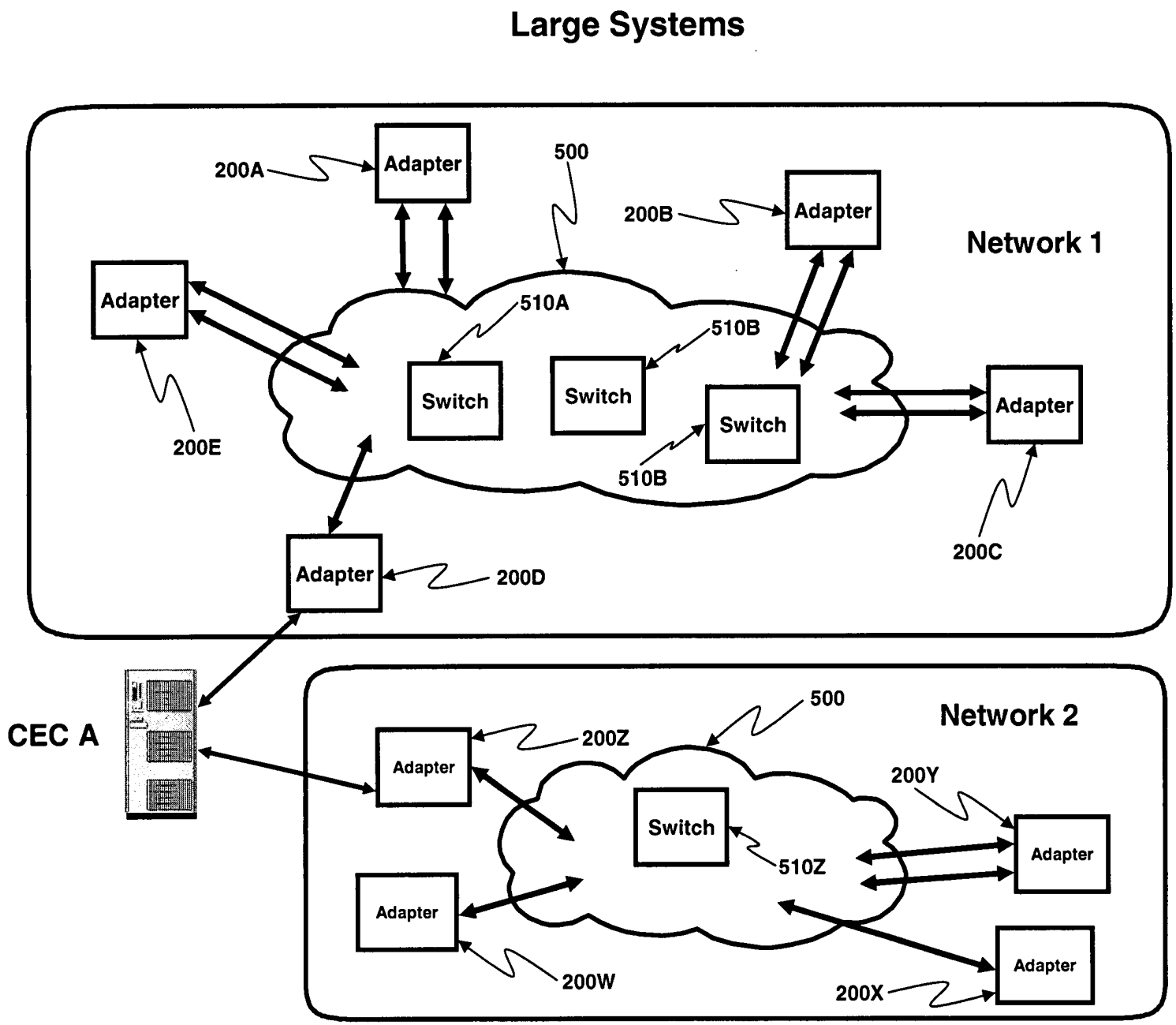

Figure 2

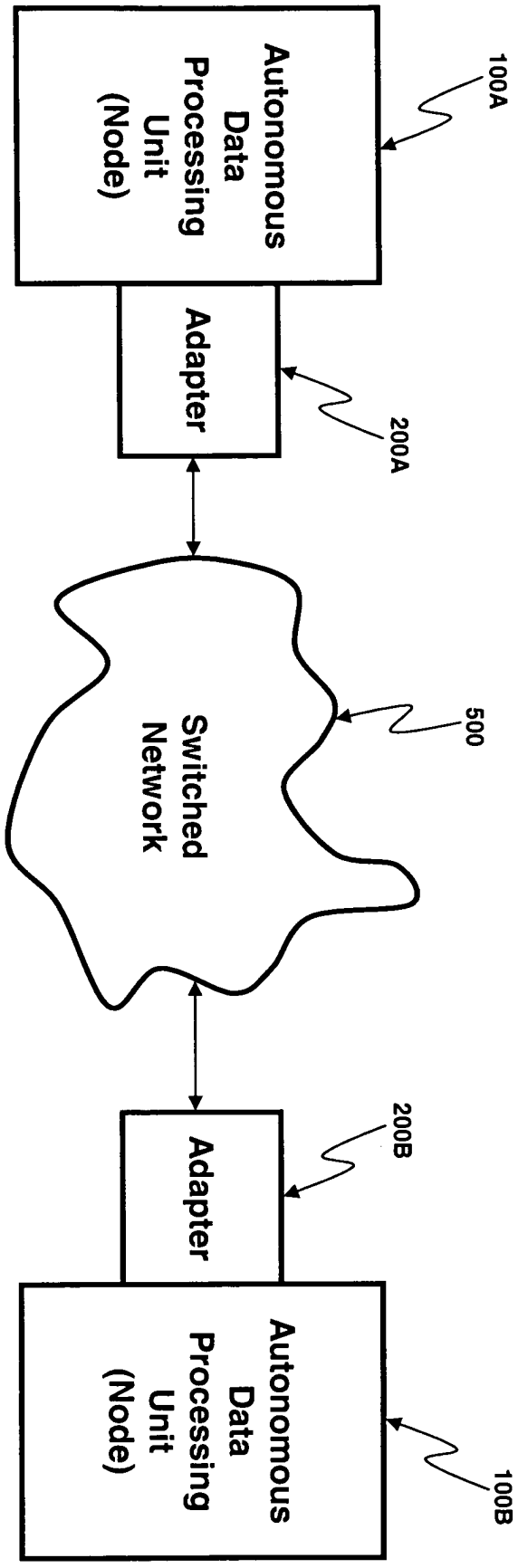
Autonomous Data Processing Unit (Node)
100A
Adapter
200A
Switched Network
500
Adapter
200B
Autonomous Data Processing Unit (Node)
100B

Figure 3

Send-Receive

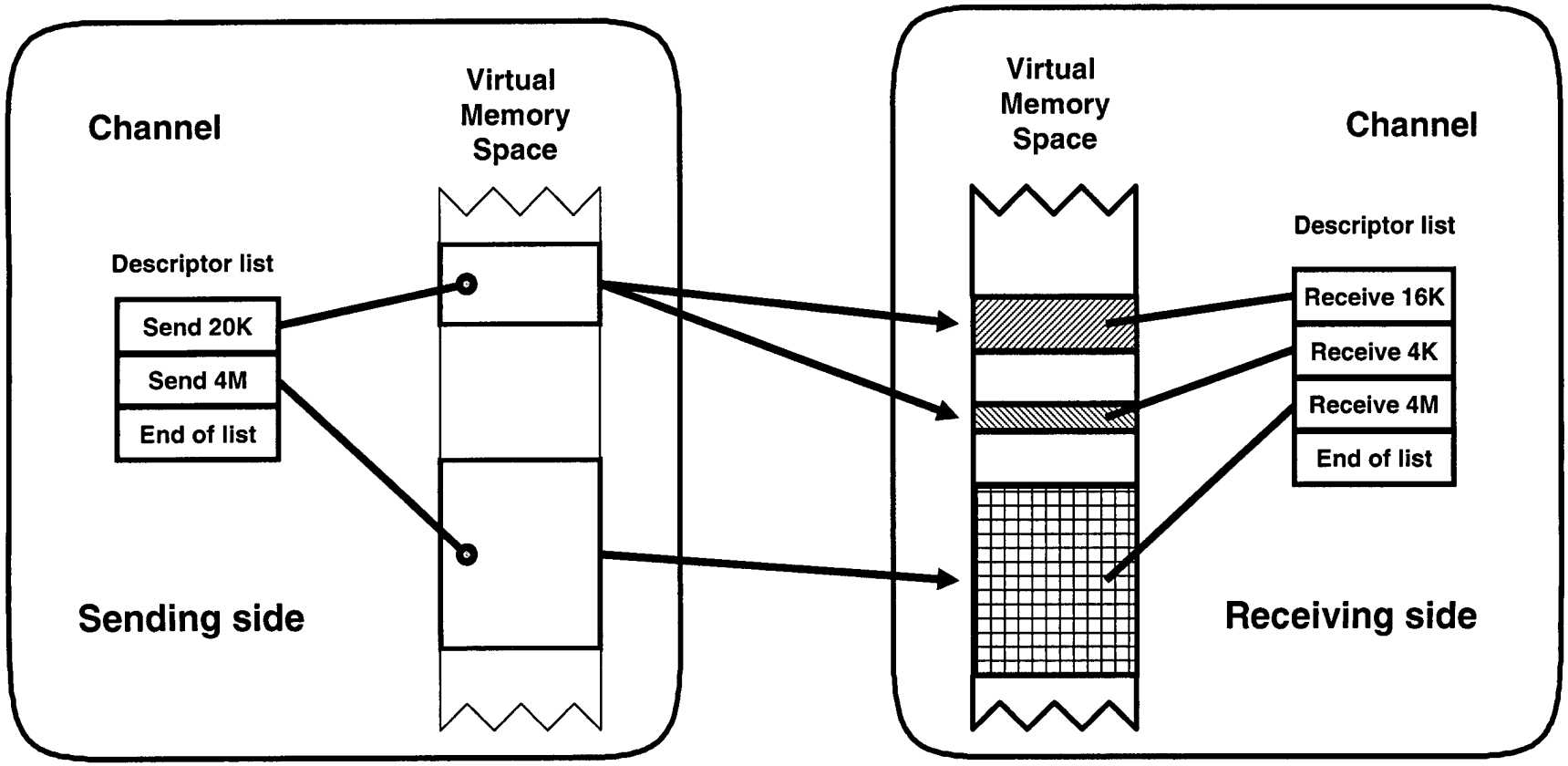

Figure 4

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Remote Read-Write

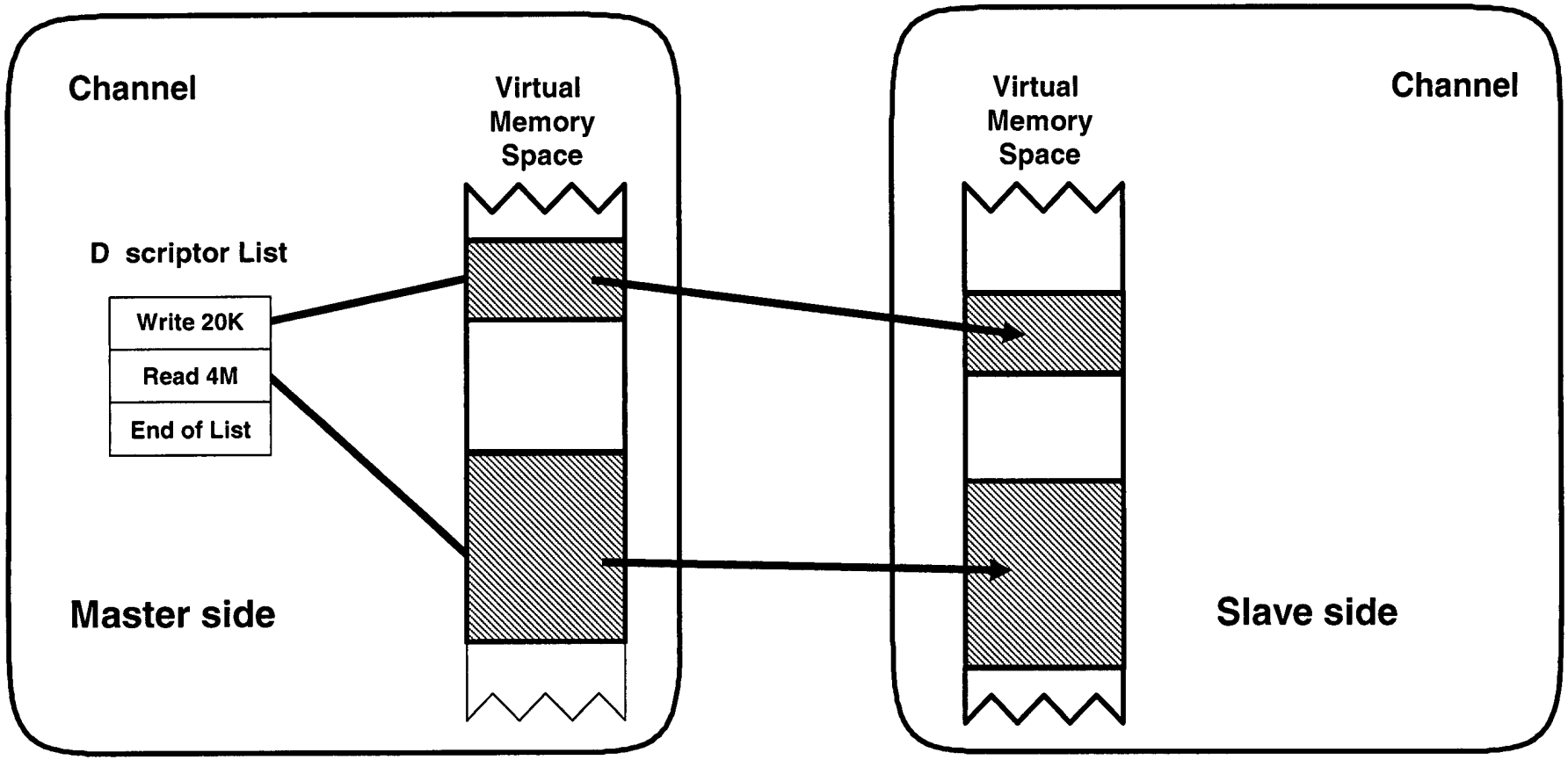

Figure 5

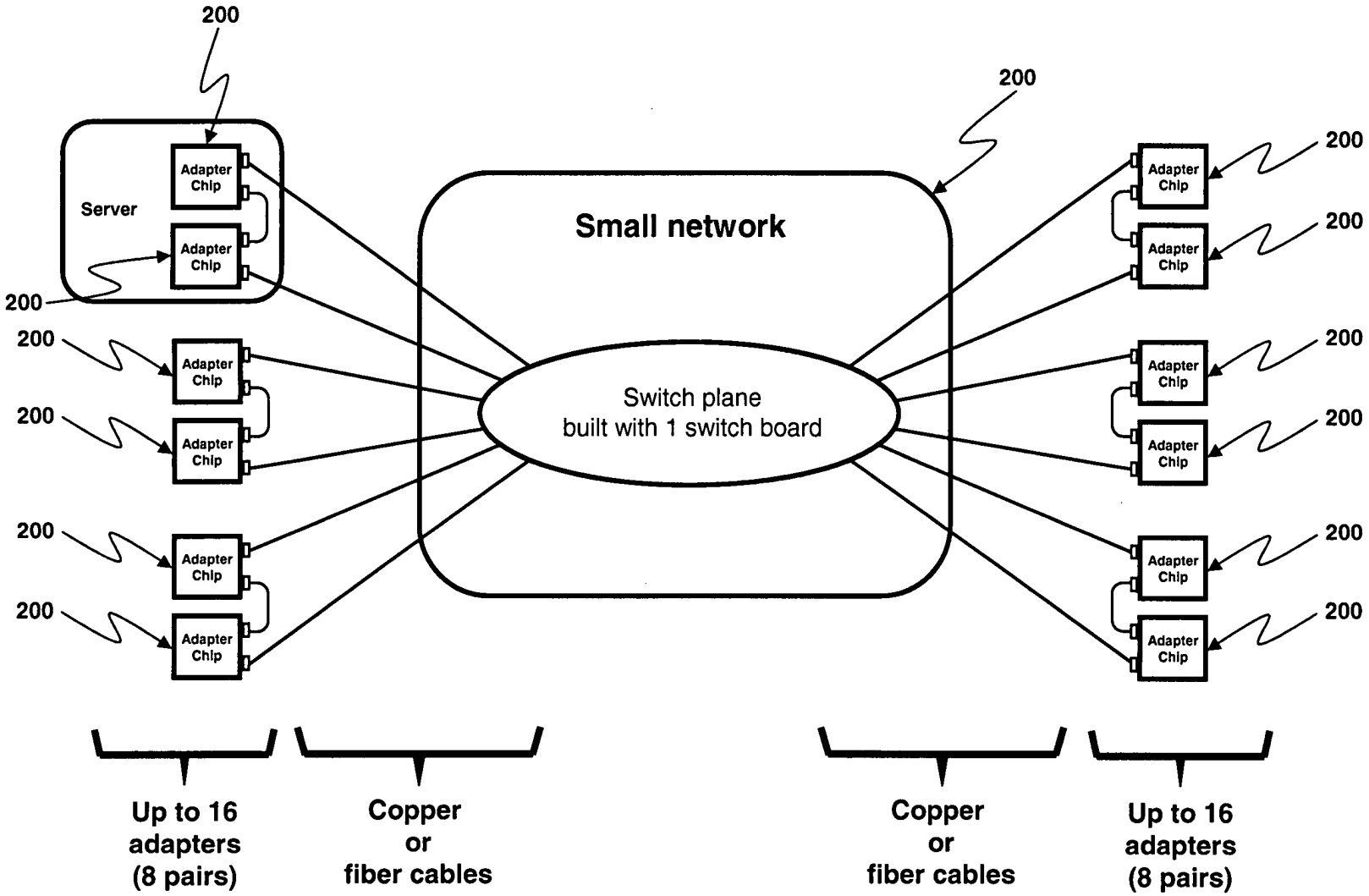
200
200
Server
Adapter Chip
Adapter Chip
200
200
Adapter Chip
Adapter Chip
200
200
Adapter Chip
Adapter Chip
Small network
Switch plane
built with 1 switch board
200
200
Adapter Chip
Adapter Chip
200
200
Adapter Chip
Adapter Chip
200
200
Adapter Chip
Adapter Chip
Up to 16 adapters (8 pairs)
Copper or fiber cables
Copper or fiber cables
Up to 16 adapters (8 pairs)

Figure 6

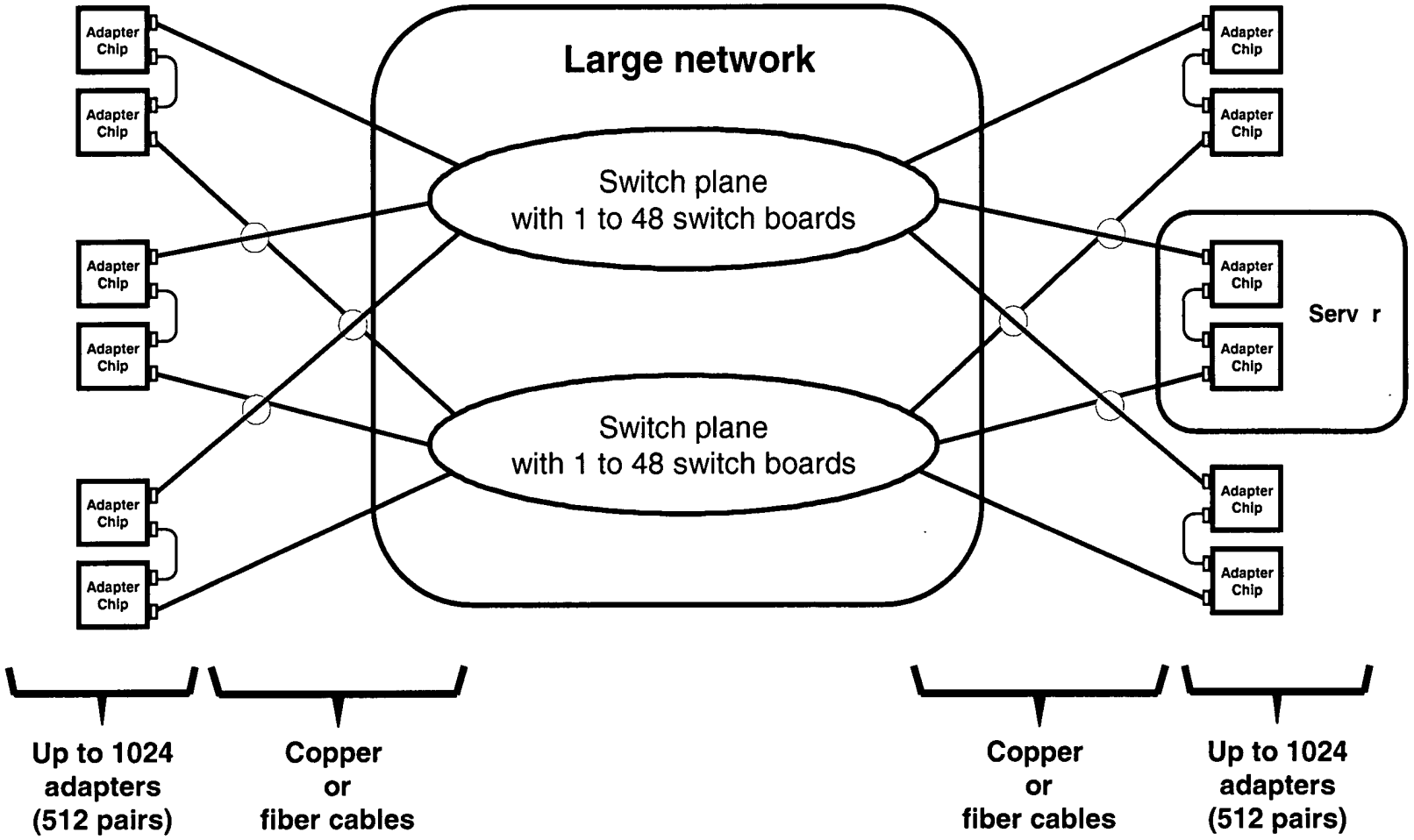
Large network
Switch plane
with 1 to 48 switch boards
Switch plane
with 1 to 48 switch boards
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Adapter Chip
Serv r
Up to 1024 adapters (512 pairs)
Copper or fiber cables
Copper or fiber cables
Up to 1024 adapters (512 pairs)

Figure 7

Programming Interface

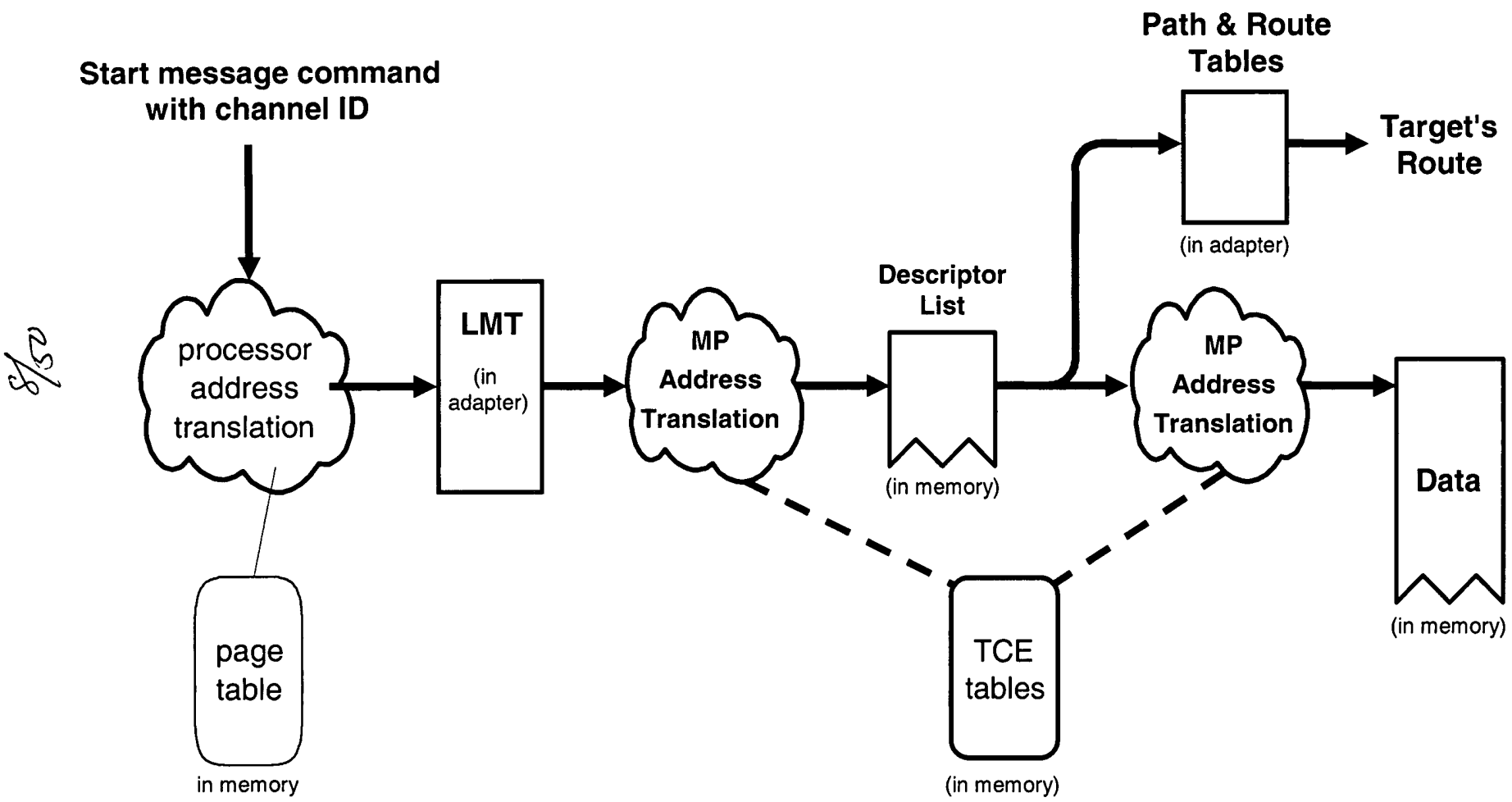

Figure 8

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Address Translation

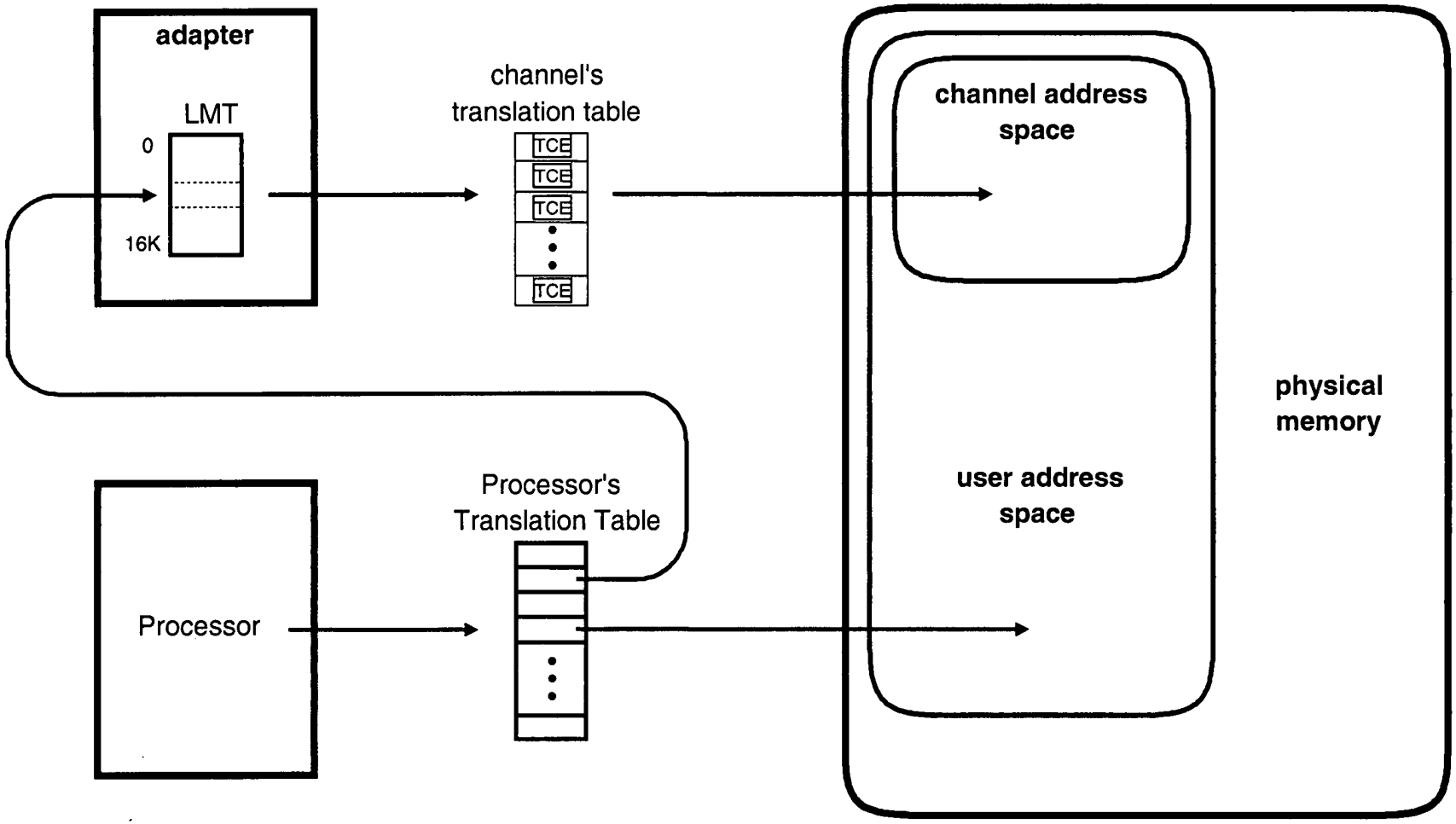


Figure 9

Address Translation with 4K pages

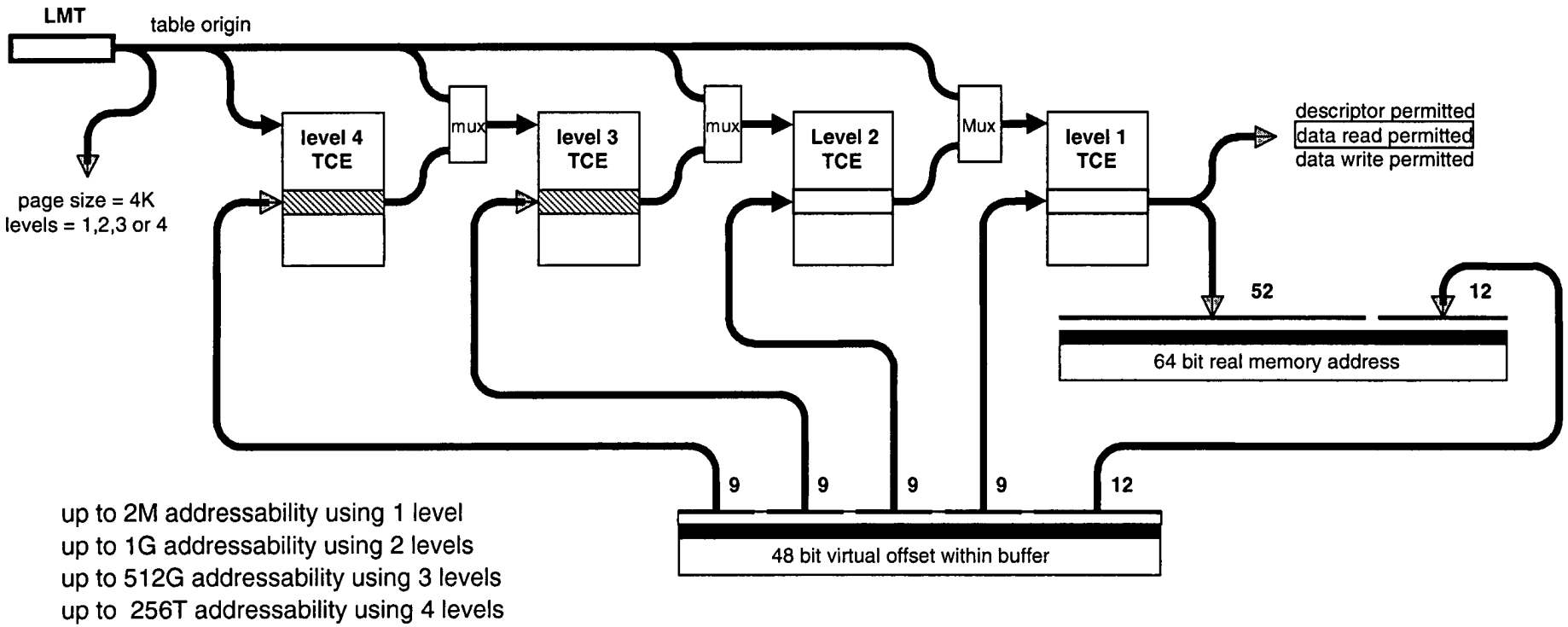
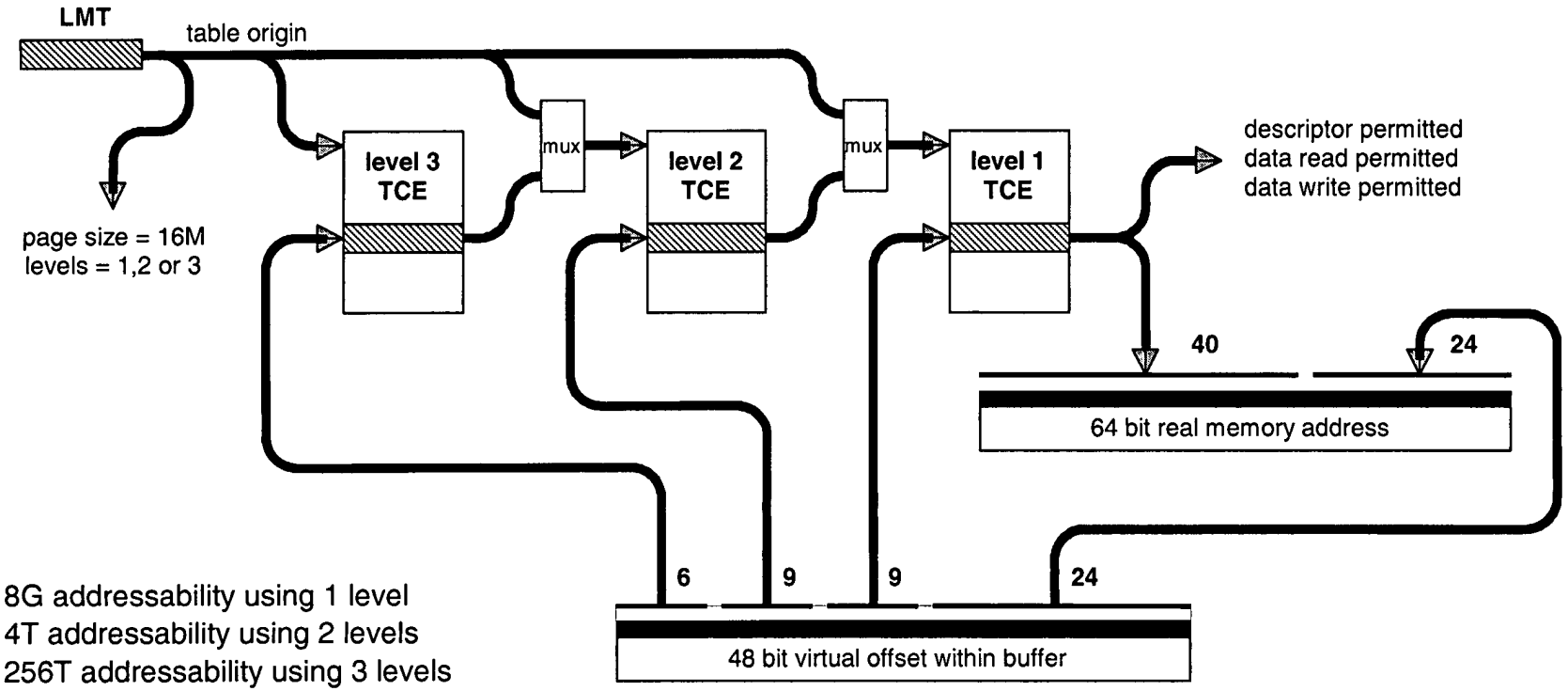


Figure 10

Address Translation with 16M pages



up to 8G addressability using 1 level
up to 4T addressability using 2 levels
up to 256T addressability using 3 levels

Figure 11

Adapter Identification

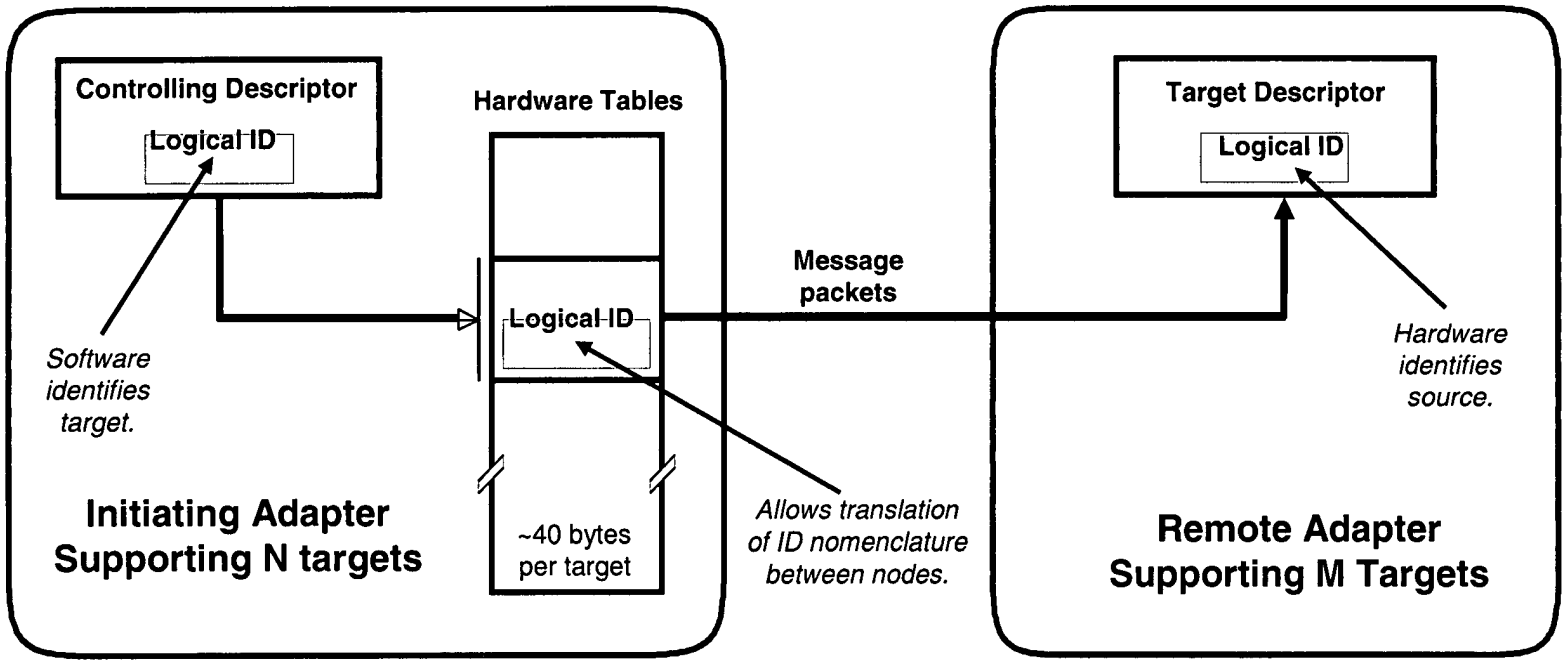


Figure 12

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Broadcast Function

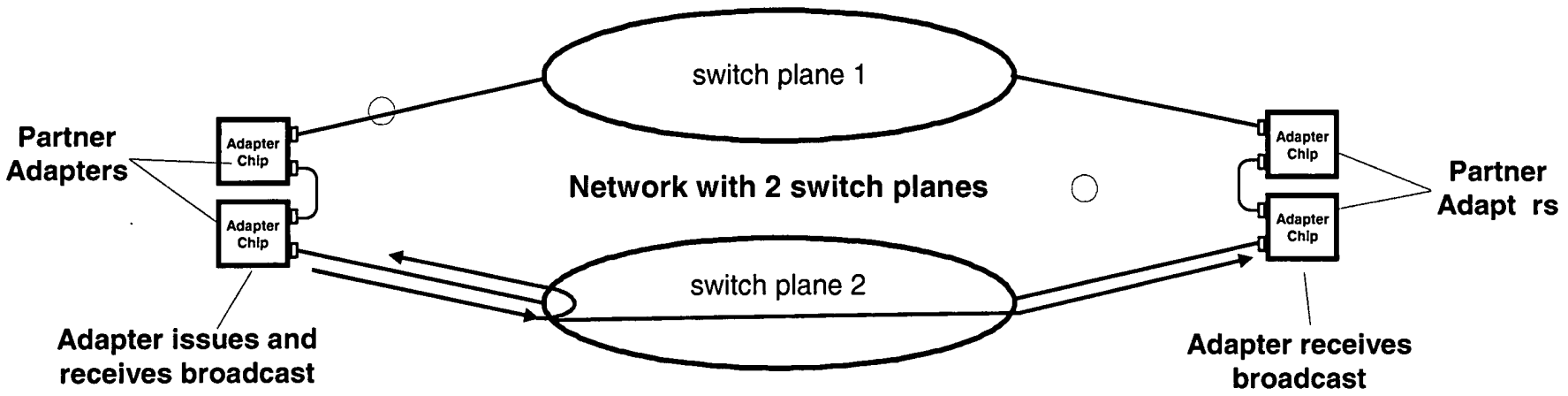

Figure 13

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Processor Interrupts

Channel Interrupt Generation

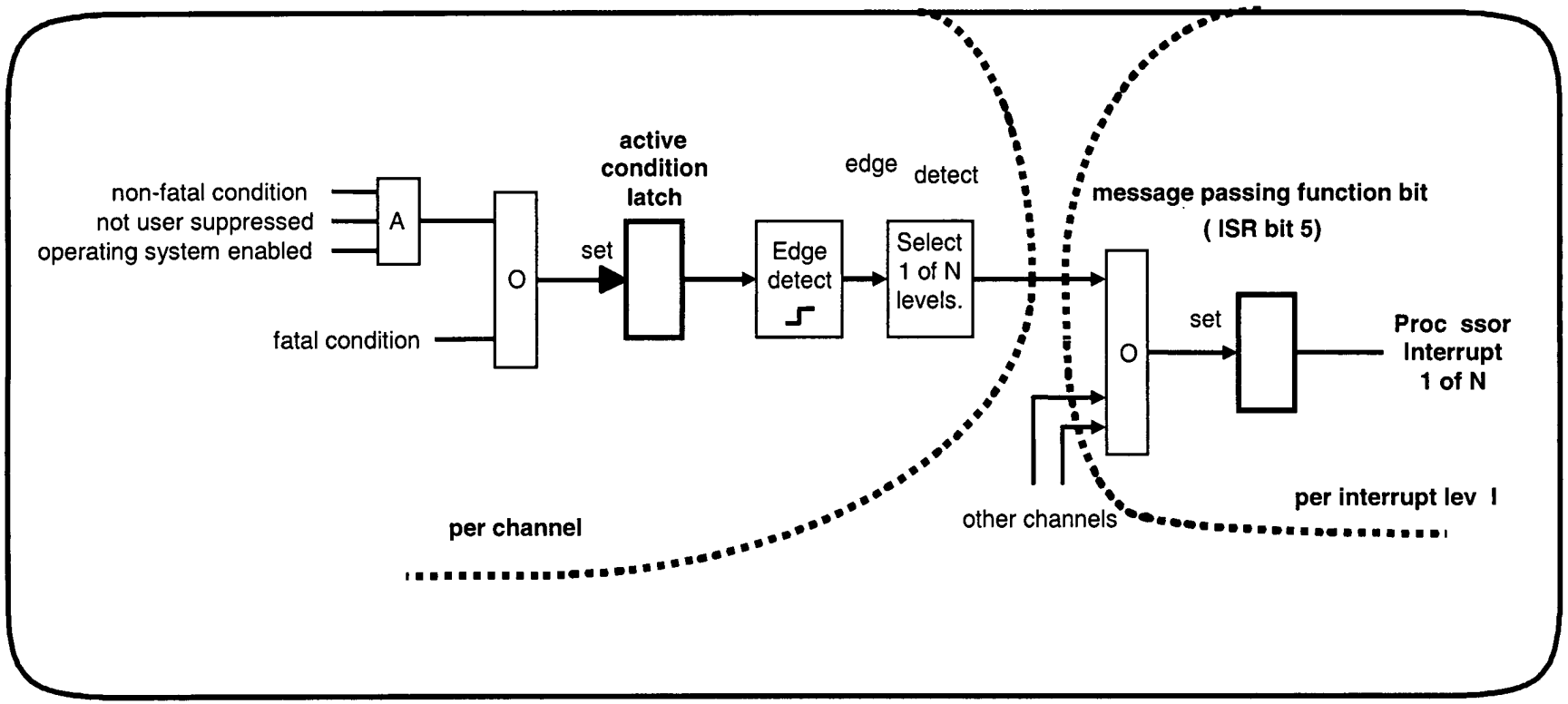

Figure 14

Defined Address Fields

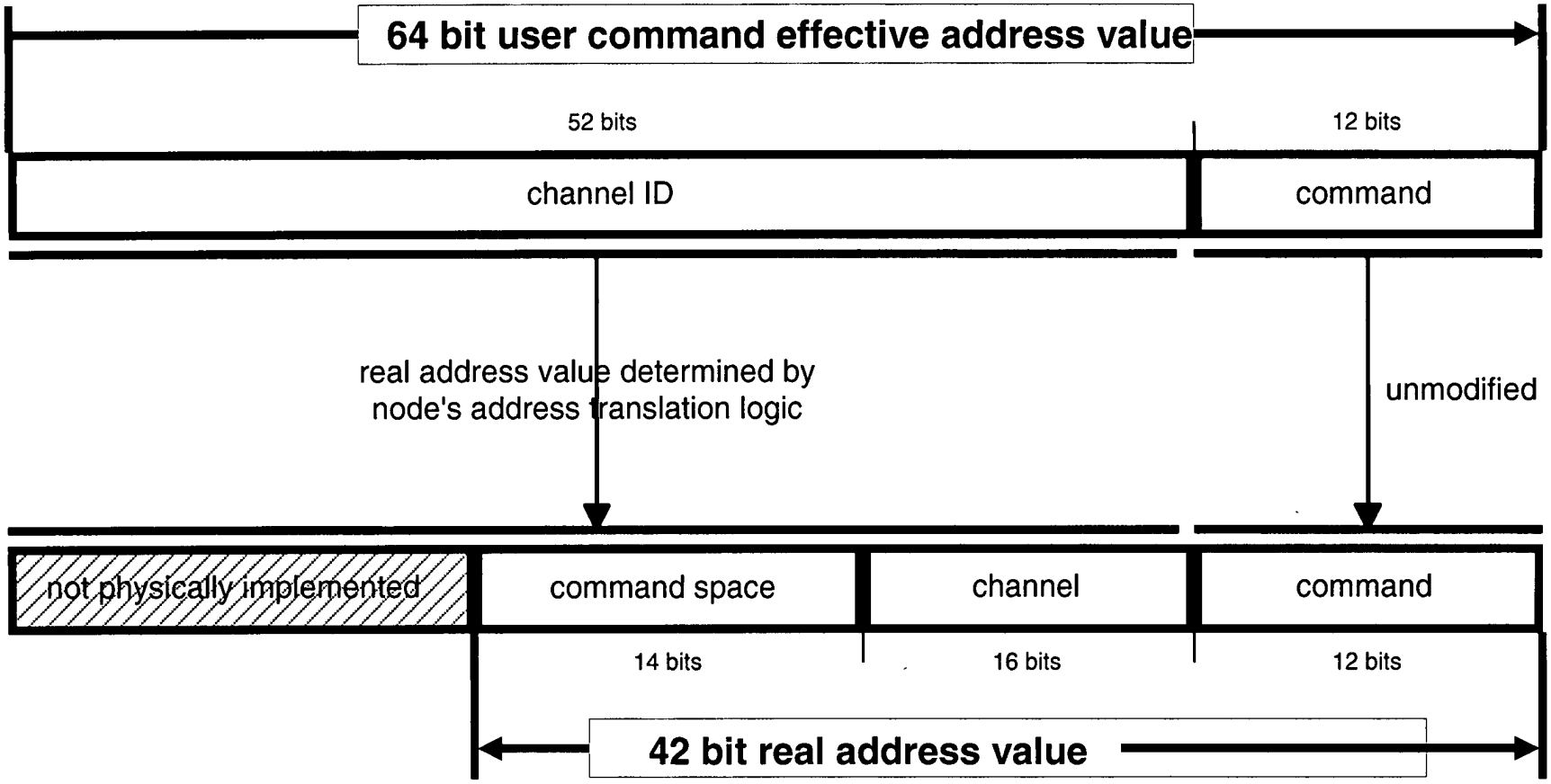

Figure 15

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Channel States

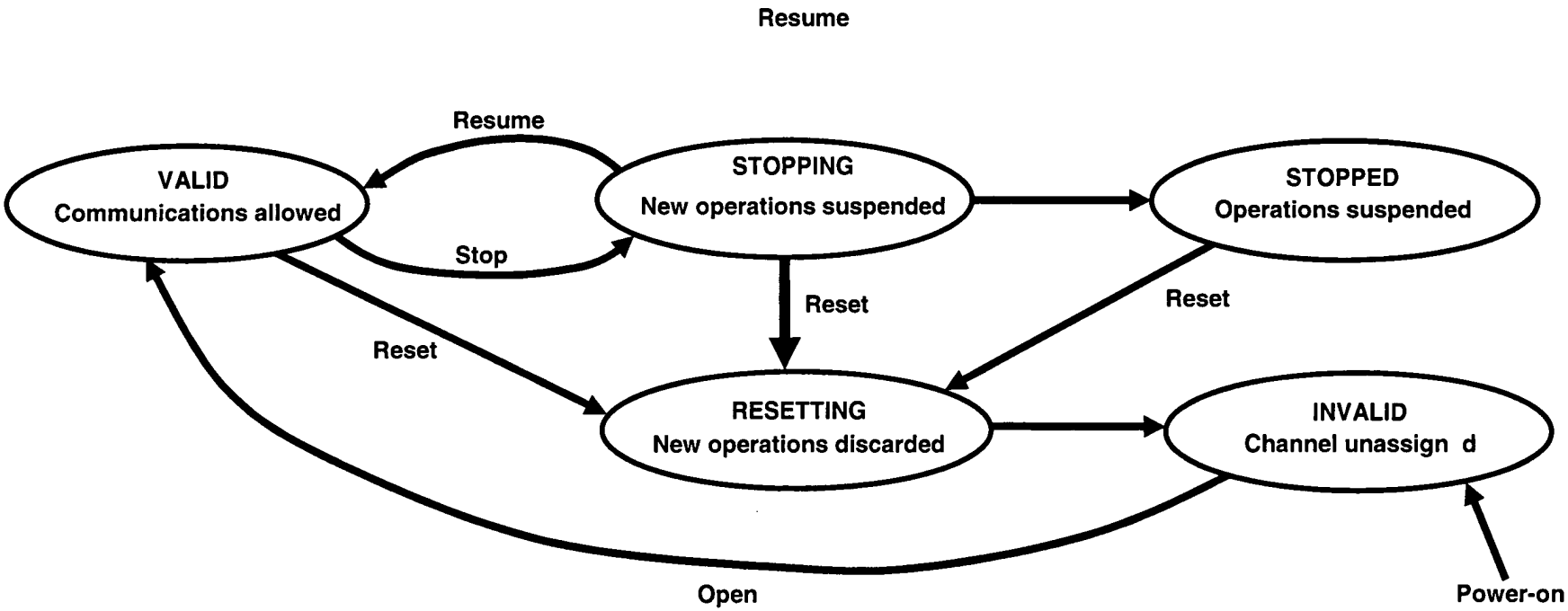

Figure 16

Local Mapping Table (LMT) Entries

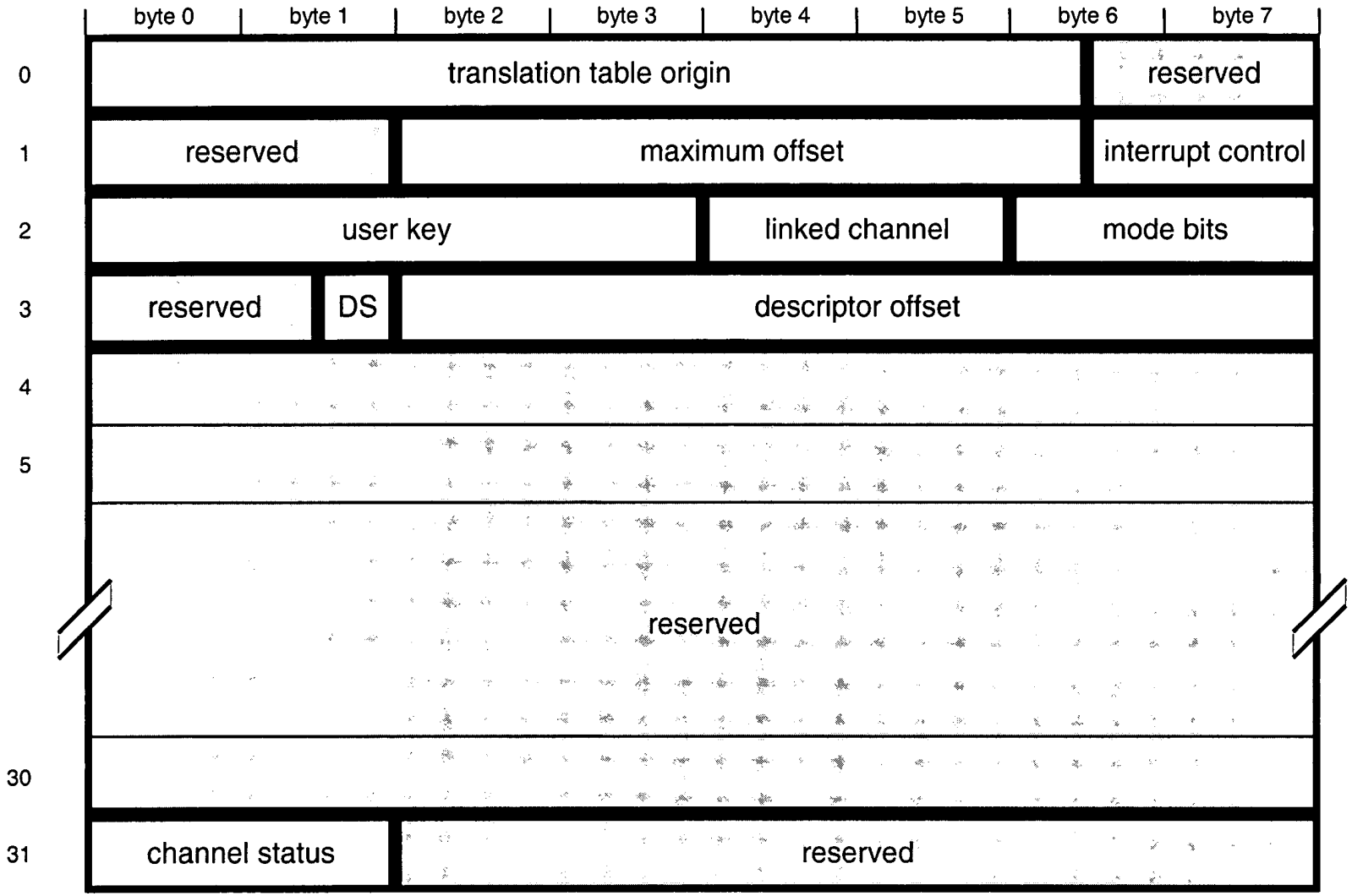

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Figure 17

Translation Control Elements

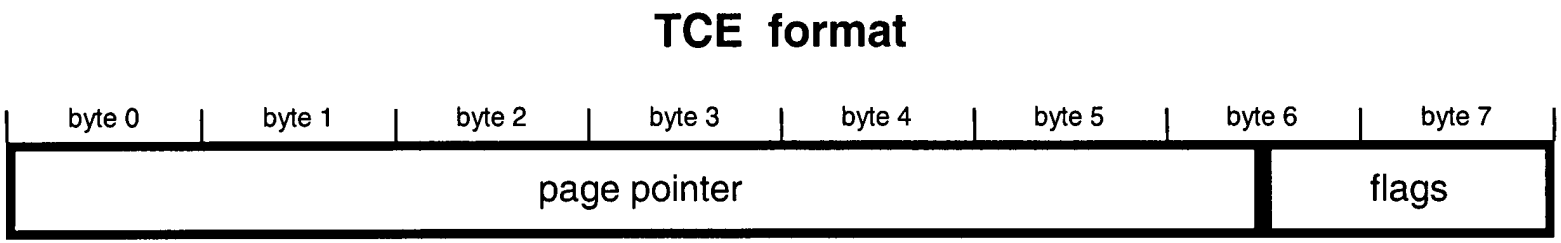

Figure 18

Remote Write

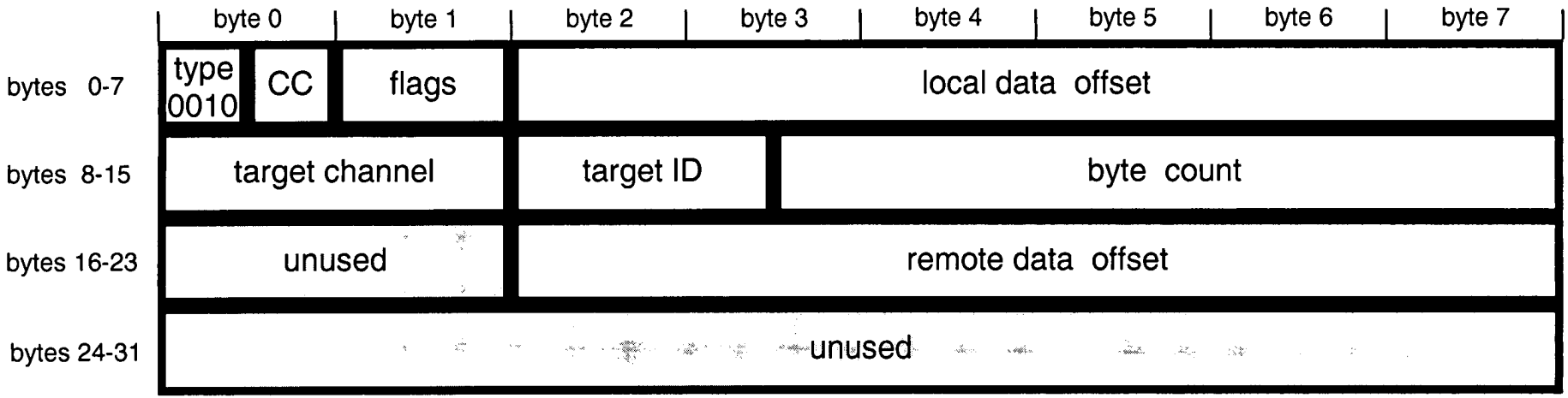

Figure 19

Remote Read

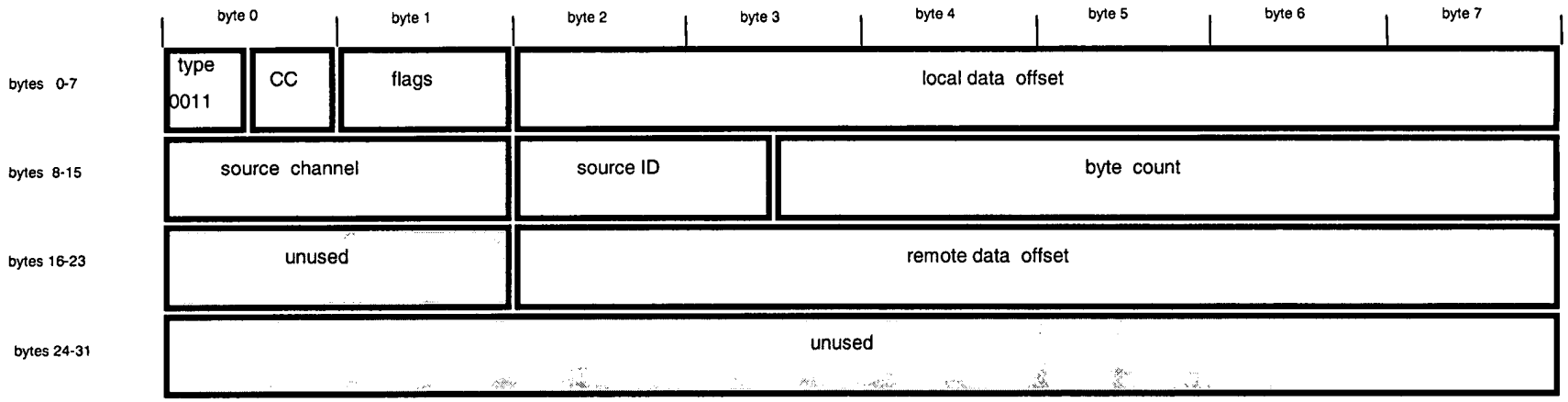

Figure 20

Source of Push

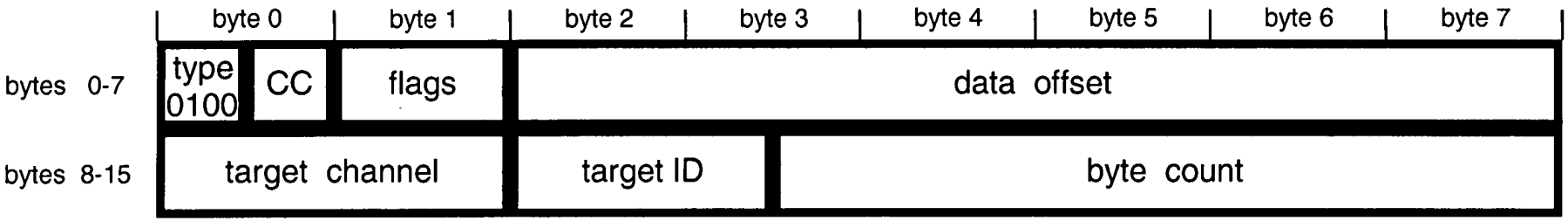

Figure 21

Target of push

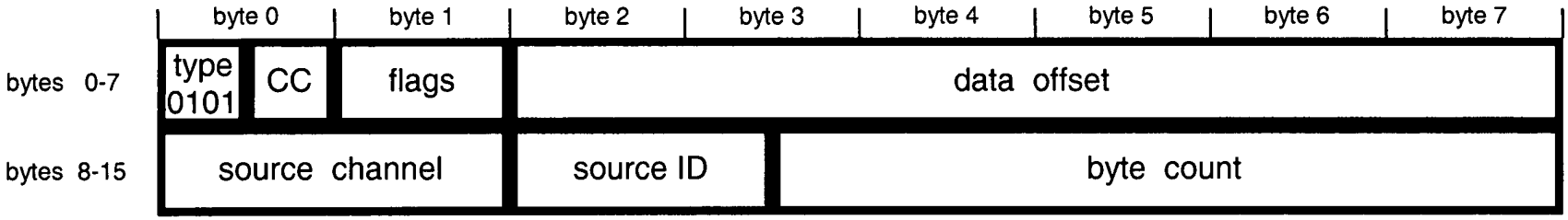

Figure 22

Source of Pull

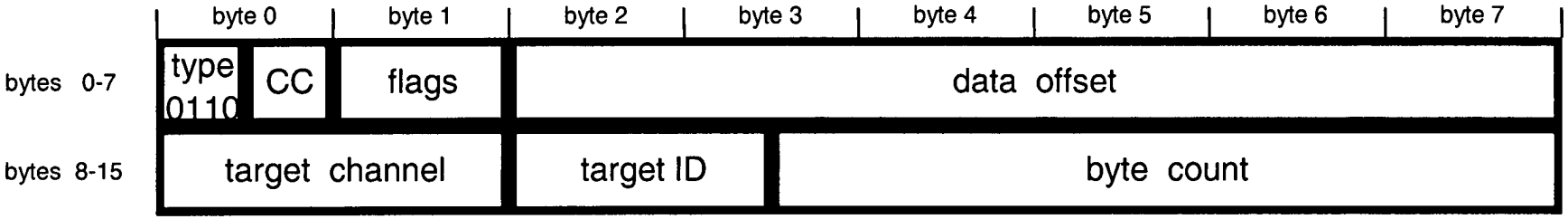

Figure 23

Target of pull

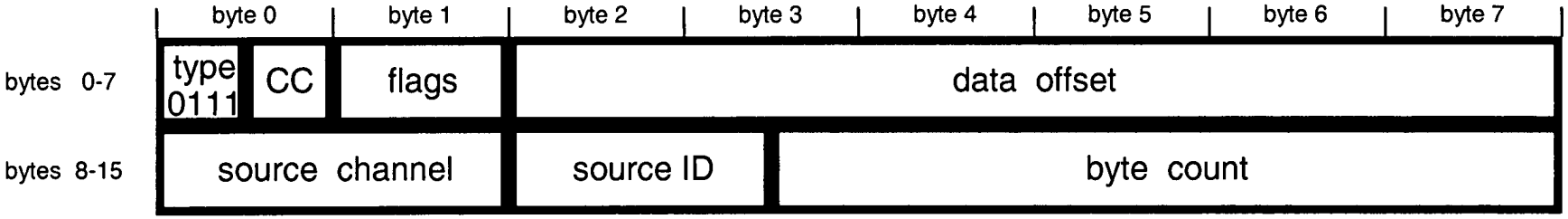

Figure 24

2575

Preload data

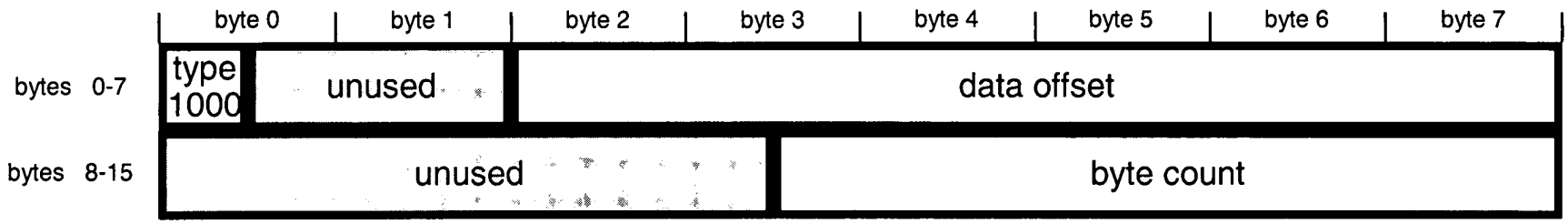

Figure 25

Branch

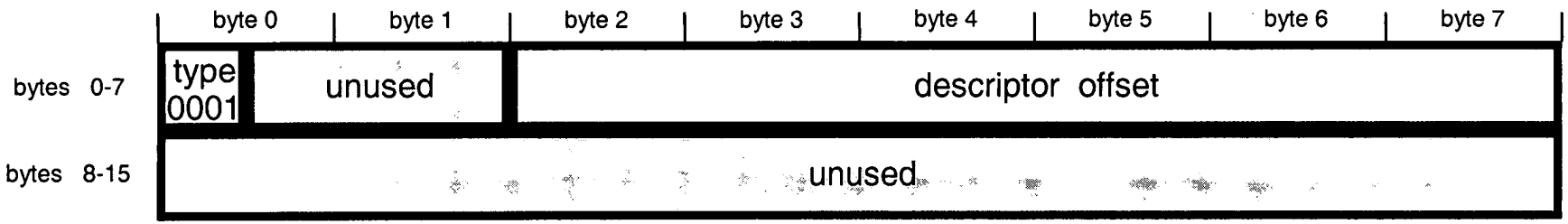

Figure 26

Path Table Entry

Figure 27

Route Table Entry

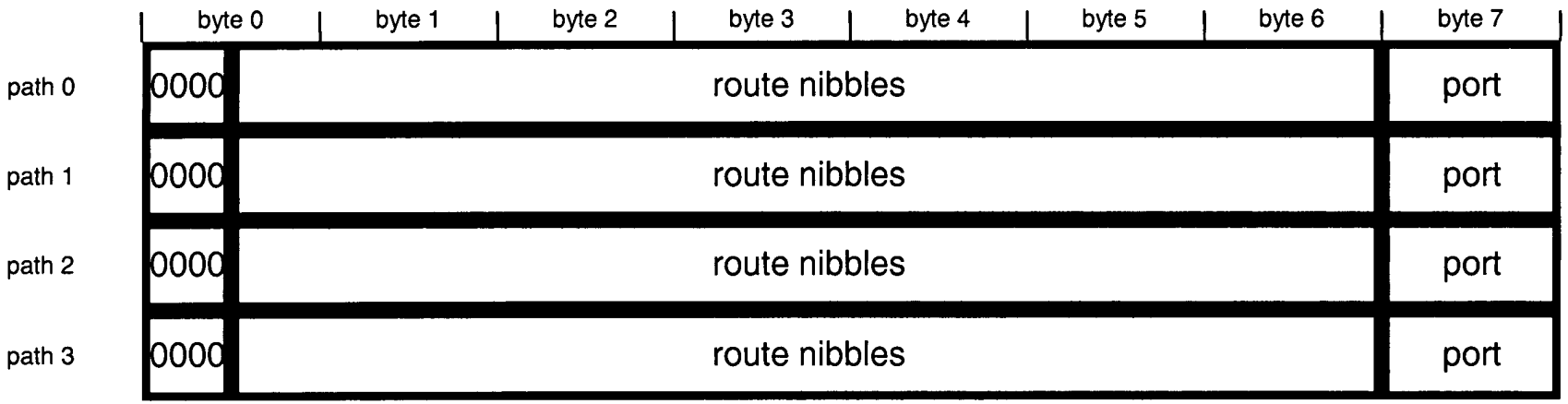

Figure 28

Broadcast Registers

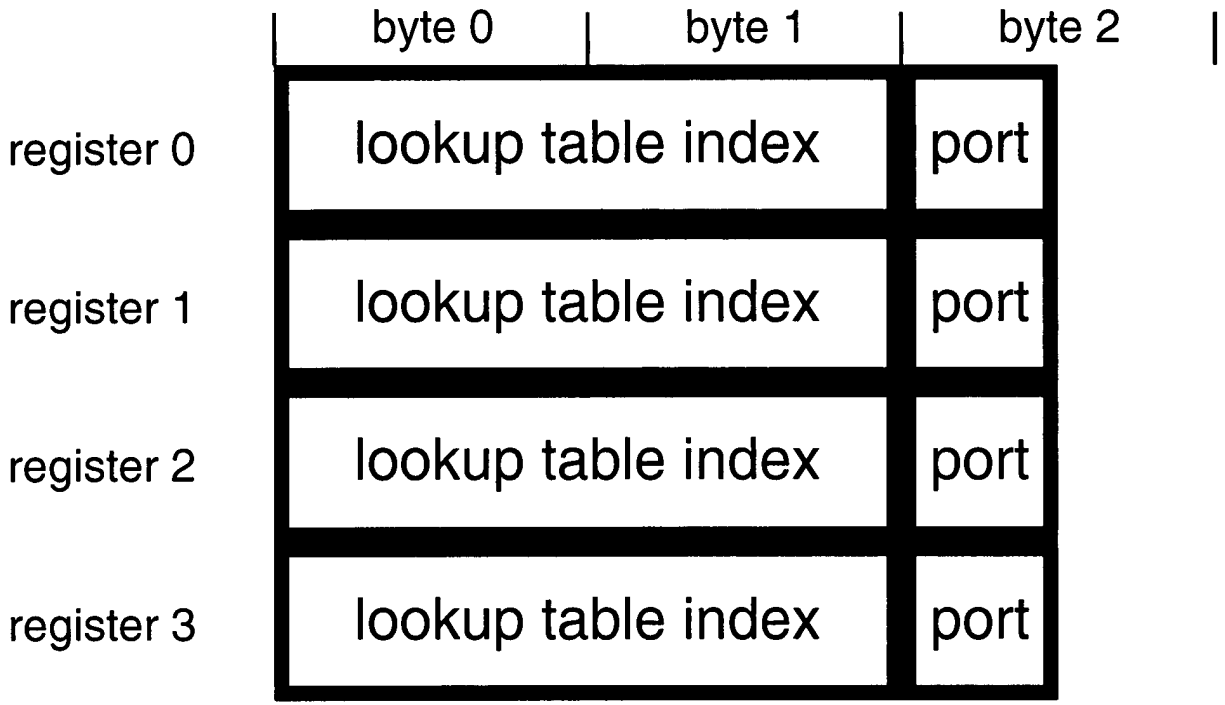

Figure 29

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Sequence Table Entry

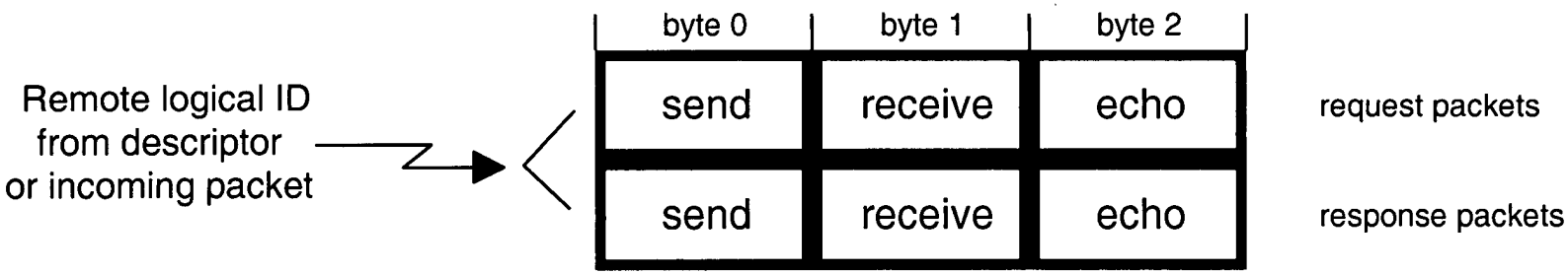

Figure 30

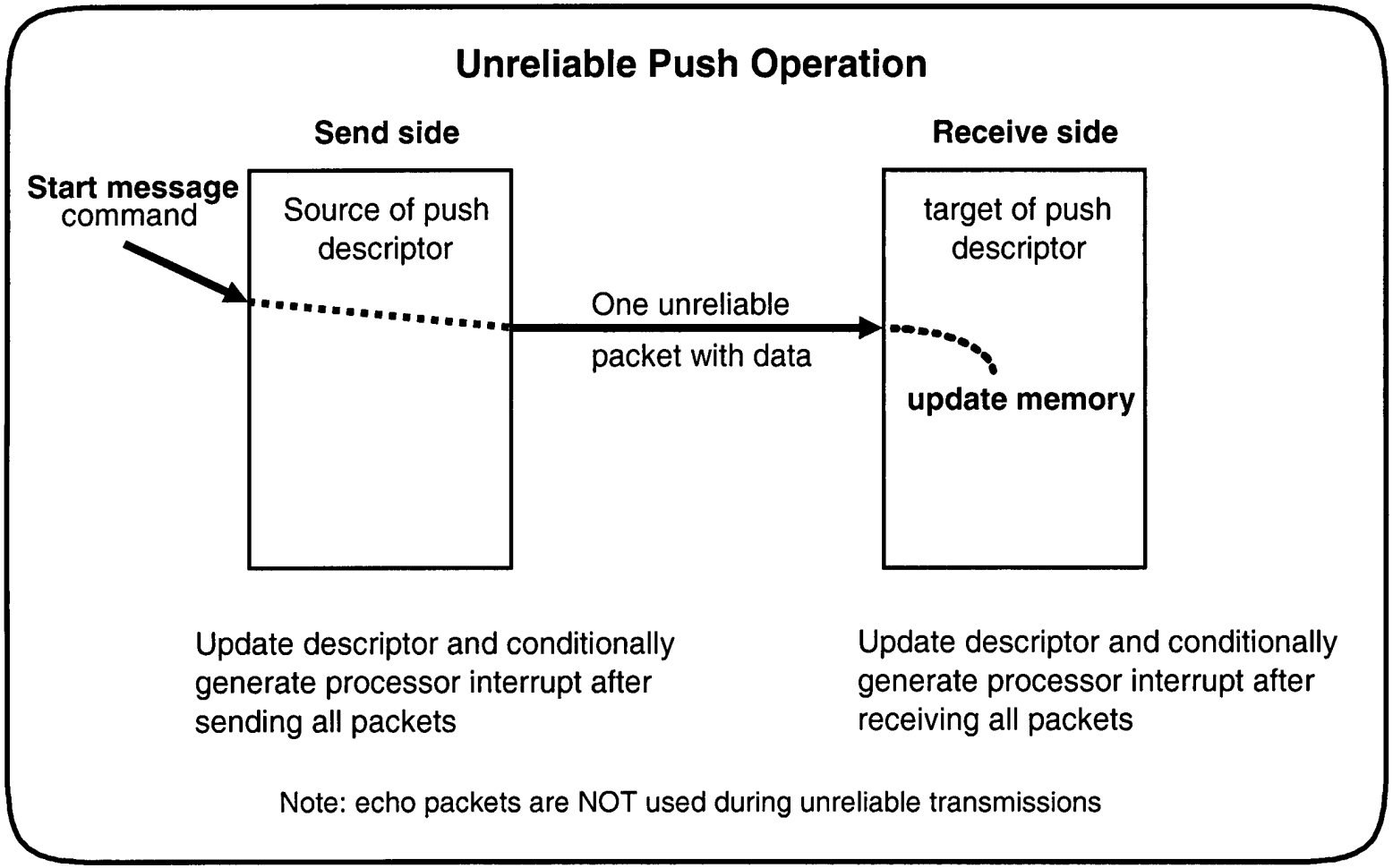
Unreliable Push Operation
Send side
Receive side
Start message command
Source of push descriptor
target of push descriptor
One unreliable packet with data
update memory
Update descriptor and conditionally generate processor interrupt after sending all packets
Update descriptor and conditionally generate processor interrupt after receiving all packets
Note: echo packets are NOT used during unreliable transmissions

Figure 31

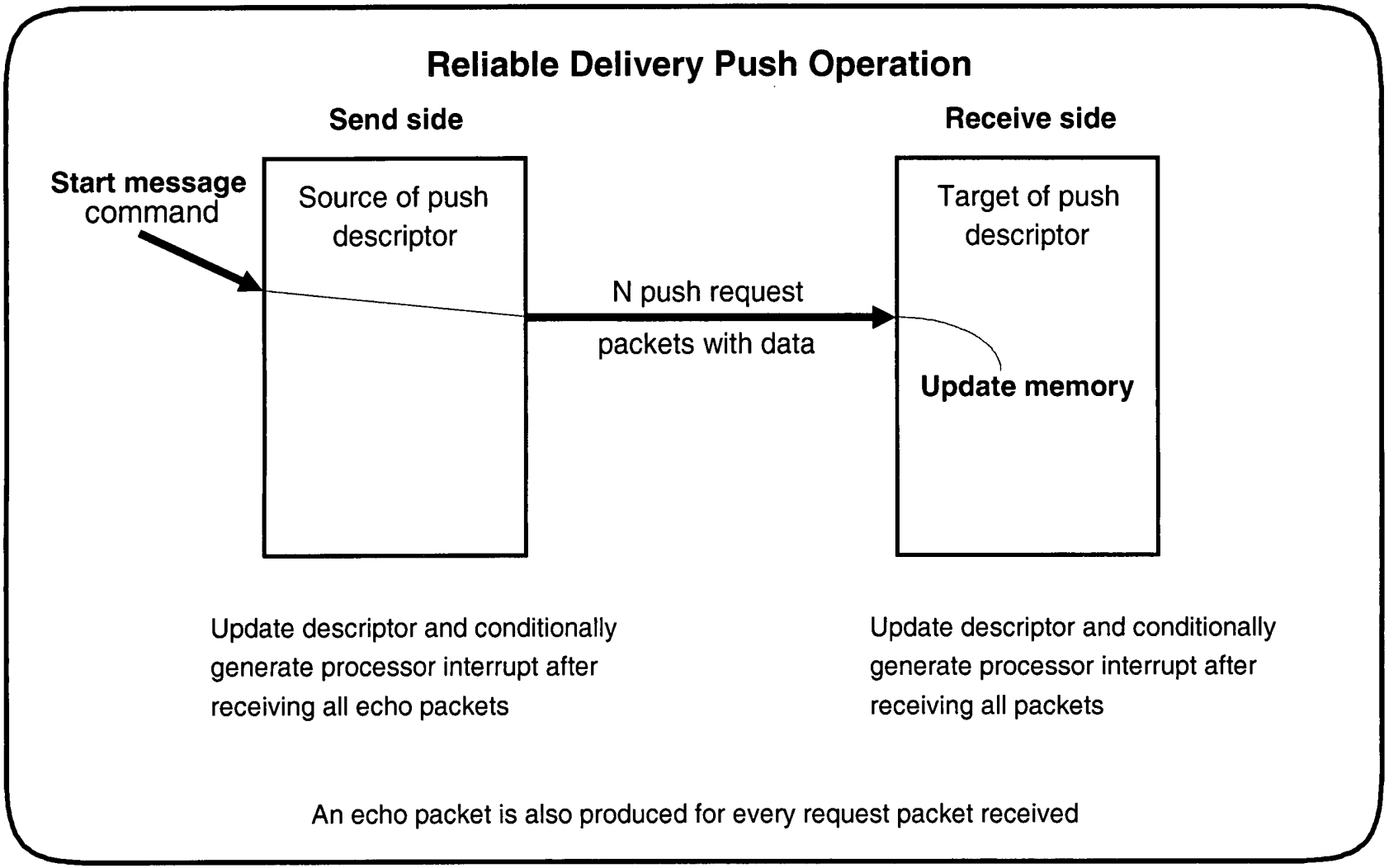
Reliable Delivery Push Operation
Send side
Receive side
Start message command
Source of push descriptor
Target of push descriptor
N push request
packets with data
Update memory
Update descriptor and conditionally generate processor interrupt after receiving all echo packets
Update descriptor and conditionally generate processor interrupt after receiving all packets
An echo packet is also produced for every request packet received

Figure 32

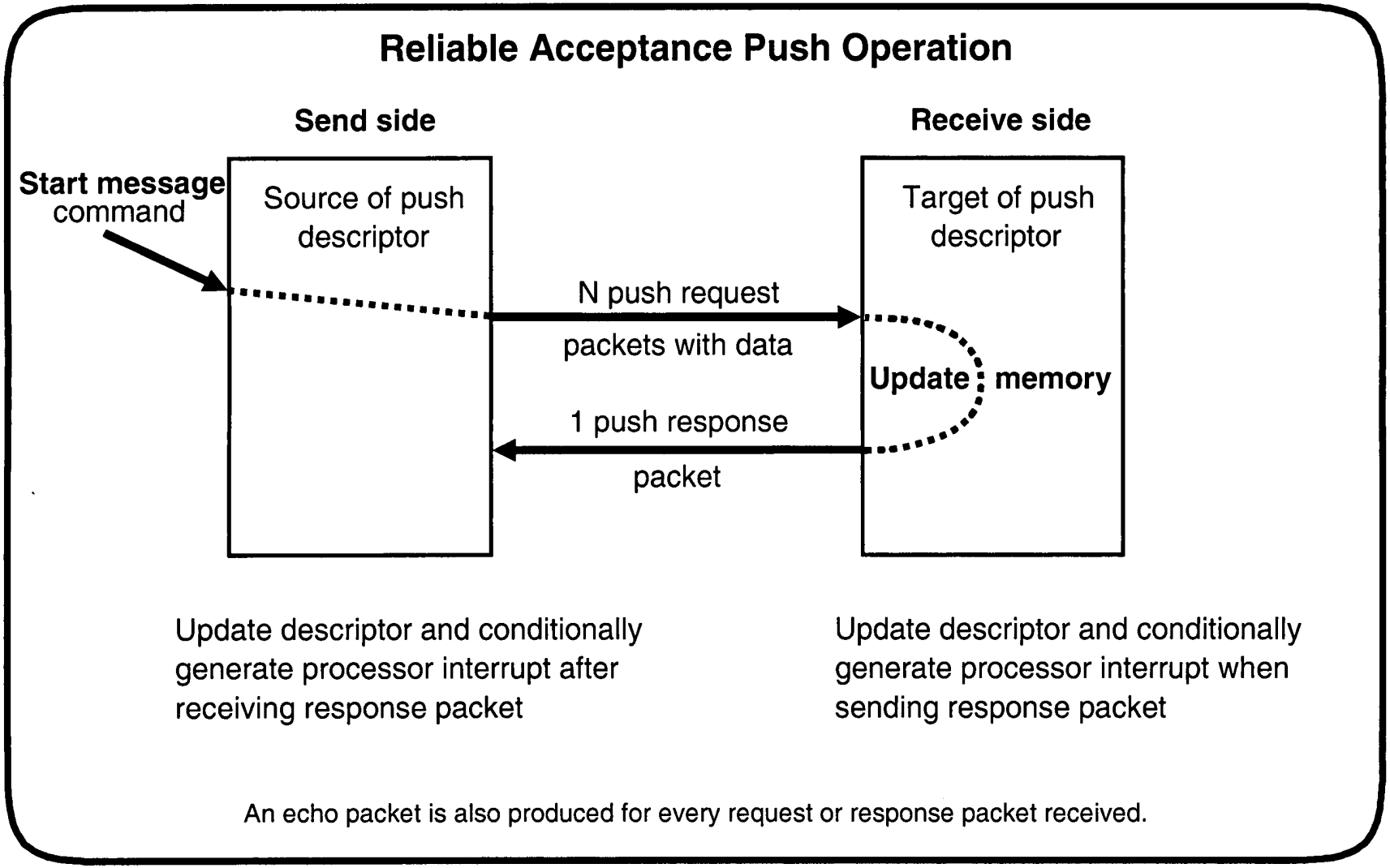
Reliable Acceptance Push Operation
Send side
Receive side
Start message command
Source of push descriptor
Target of push descriptor
N push request packets with data
Update memory
1 push response packet
Update descriptor and conditionally generate processor interrupt after receiving response packet
Update descriptor and conditionally generate processor interrupt when sending response packet
An echo packet is also produced for every request or response packet received.

Figure 33

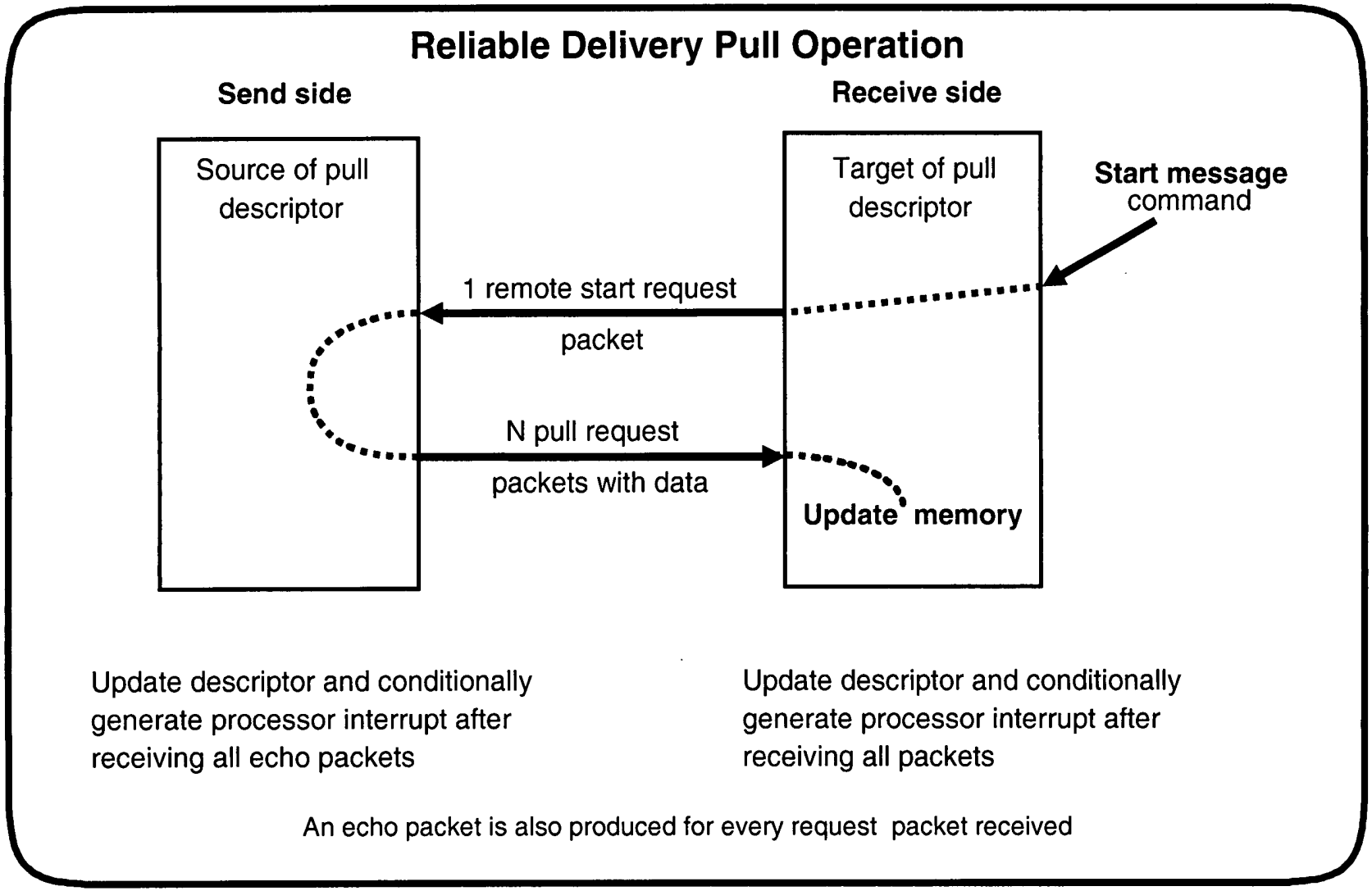
Reliable Delivery Pull Operation
Send side
Receive side
Source of pull descriptor
Target of pull descriptor
Start message command
1 remote start request packet
N pull request packets with data
Update memory
Update descriptor and conditionally generate processor interrupt after receiving all echo packets
Update descriptor and conditionally generate processor interrupt after receiving all packets
An echo packet is also produced for every request packet received

Figure 34

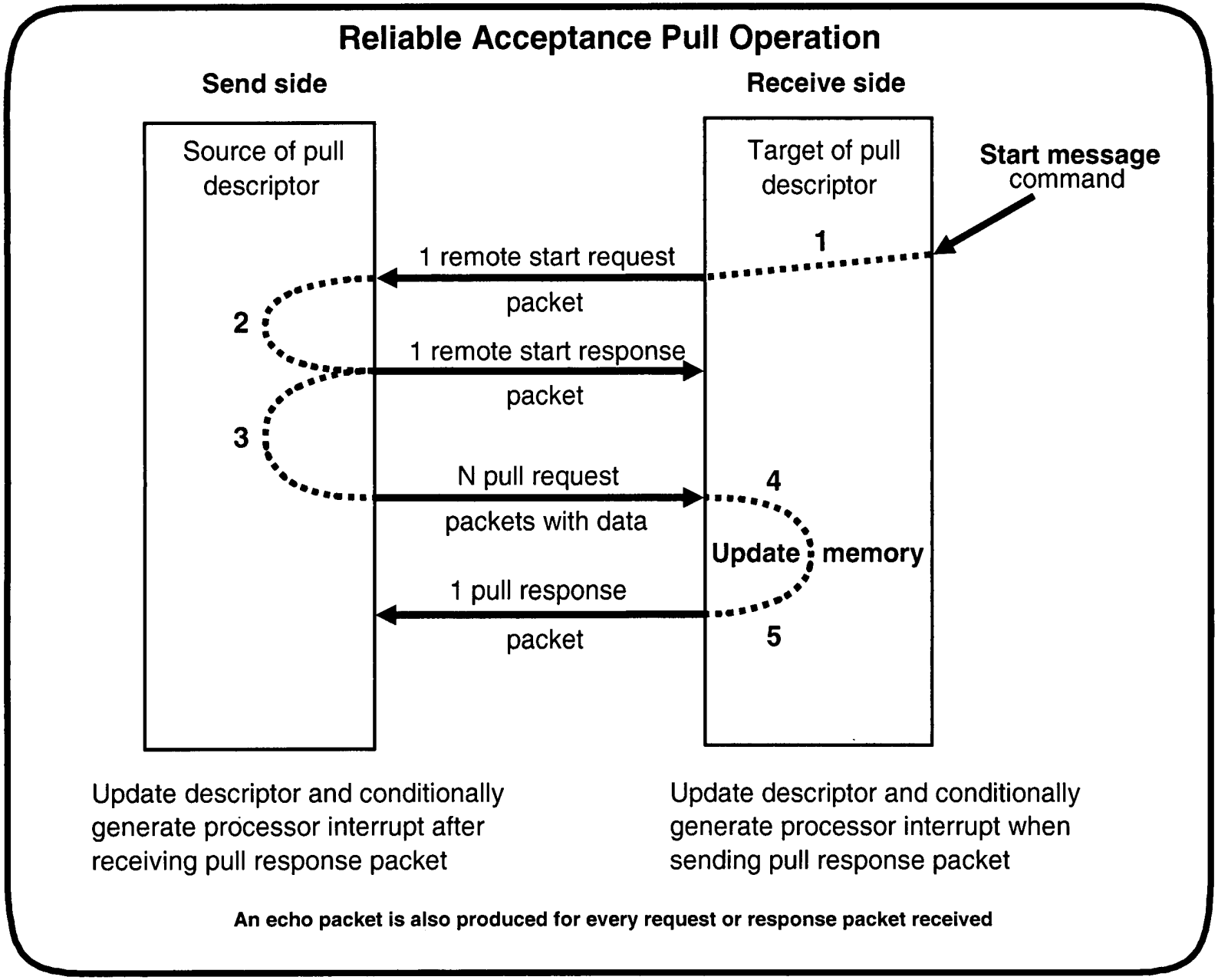
Reliable Acceptance Pull Operation
Send side
Receive side
Source of pull descriptor
Target of pull descriptor
Start message command
1
1 remote start request packet
2
1 remote start response packet
3
N pull request packets with data
4
Update memory
1 pull response packet
5
Update descriptor and conditionally generate processor interrupt after receiving pull response packet
Update descriptor and conditionally generate processor interrupt when sending pull response packet
An echo packet is also produced for every request or response packet received

Figure 35

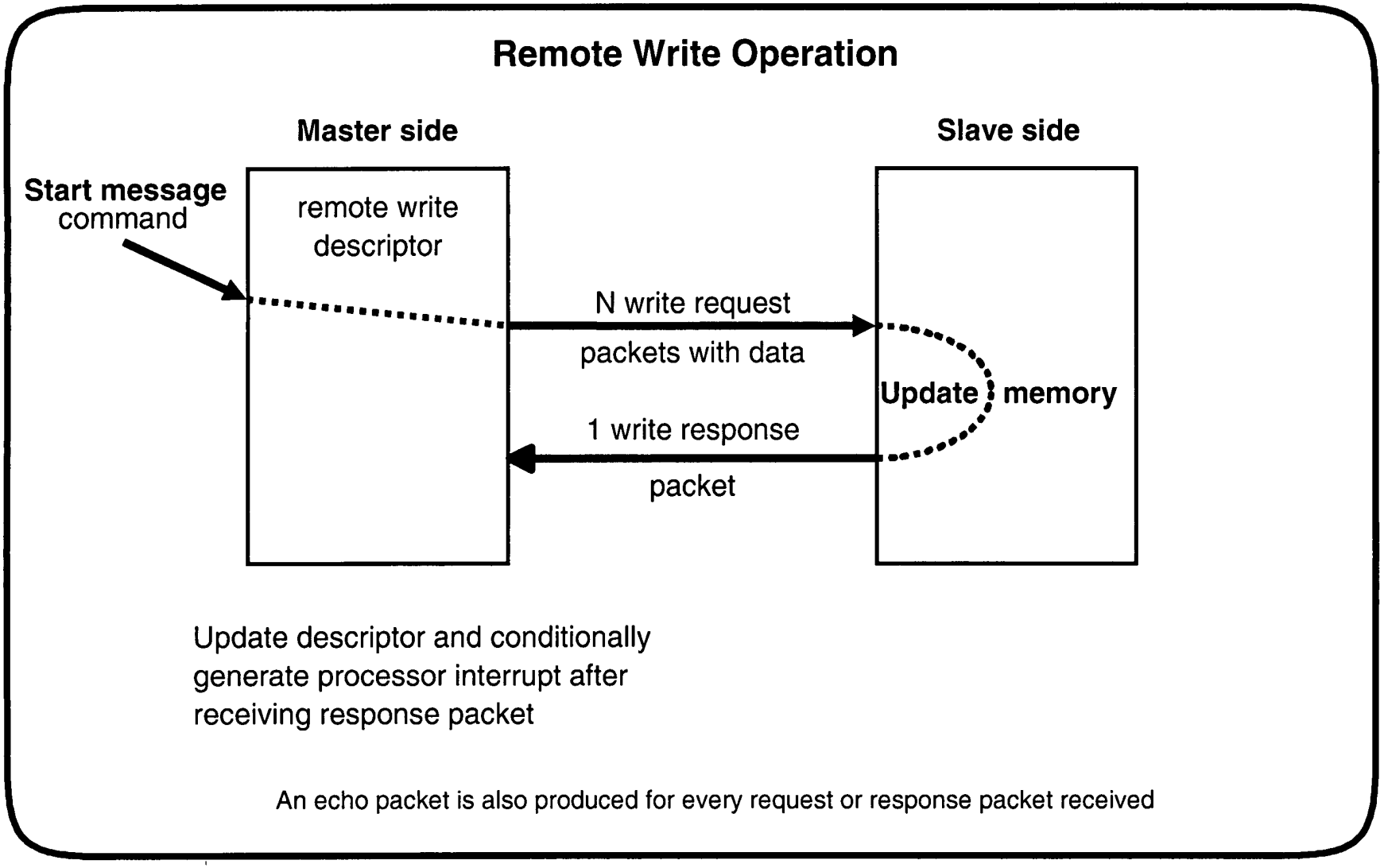
Remote Write Operation
Master side
Slave side
Start message command
remote write descriptor
N write request packets with data
Update memory
1 write response packet
Update descriptor and conditionally generate processor interrupt after receiving response packet
An echo packet is also produced for every request or response packet received

Figure 36

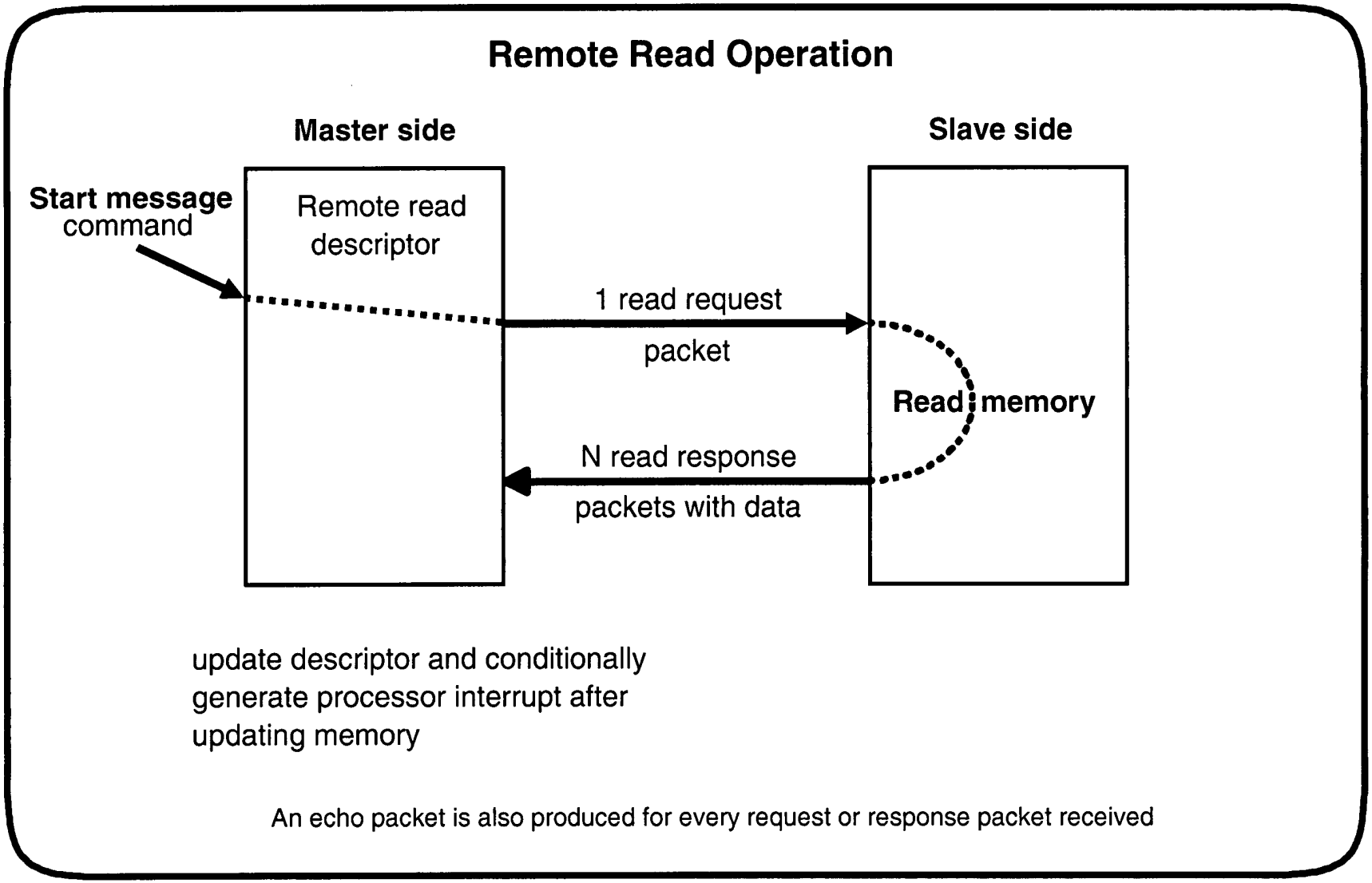
Remote Read Operation
Master side
Slave side
Start message command
Remote read descriptor
1 read request packet
Read memory
N read response packets with data
update descriptor and conditionally generate processor interrupt after updating memory
An echo packet is also produced for every request or response packet received

Figure 37

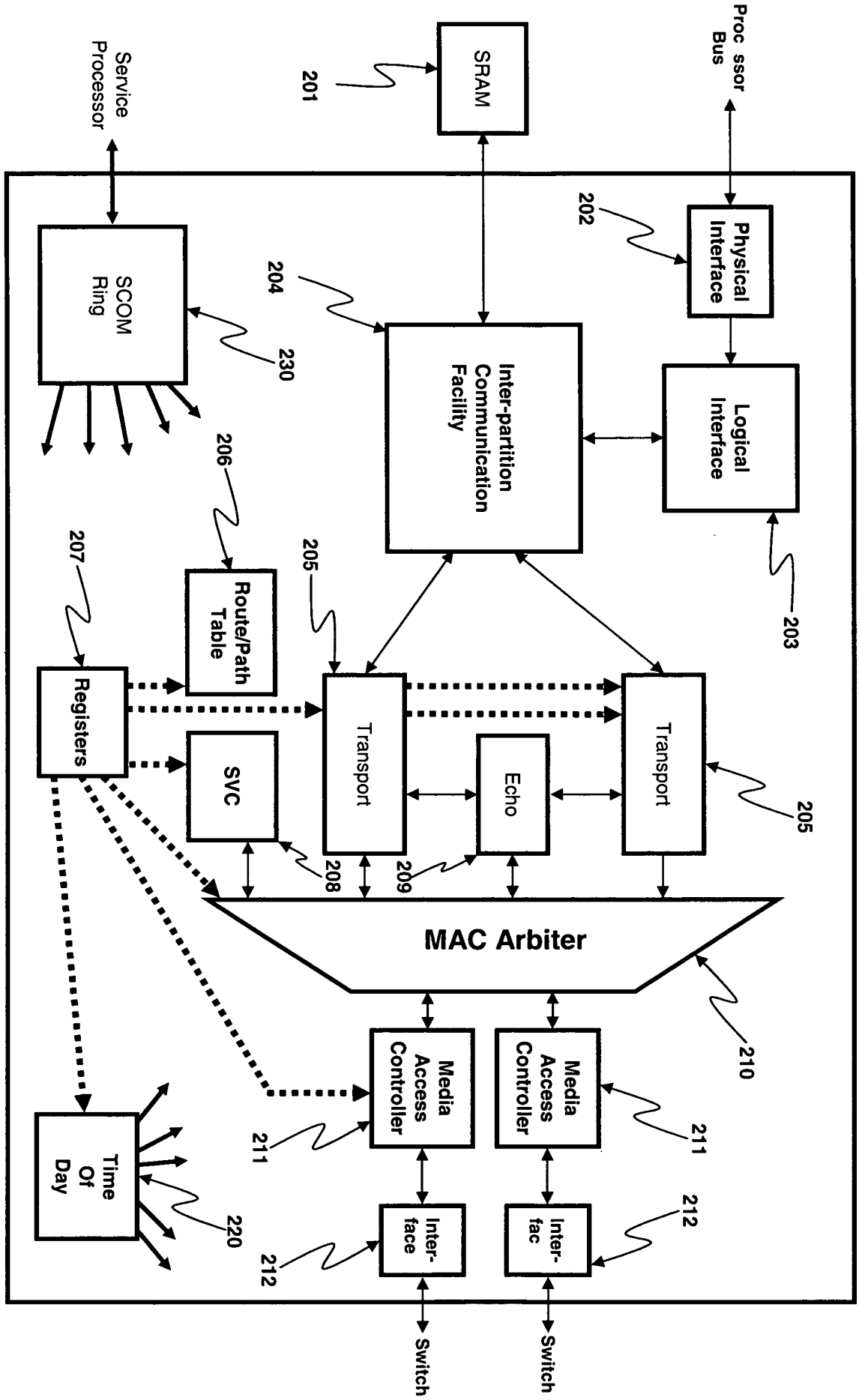
Proc ssor Bus
SRAM
201
Service Processor
200
202
Physical Interface
204
Inter-partition Communication Facility
Logical Interface
203
SCOM Ring
230
206
Route/Path Table
207
205
Registers
Transport
Transport
SVC
Echo
205
208
209
MAC Arbiter
210
Media Access Controller
Media Access Controller
211
211
Time Of Day
220
Inter-face
Inter-fac
212
212
Switch
Switch

Figure 38

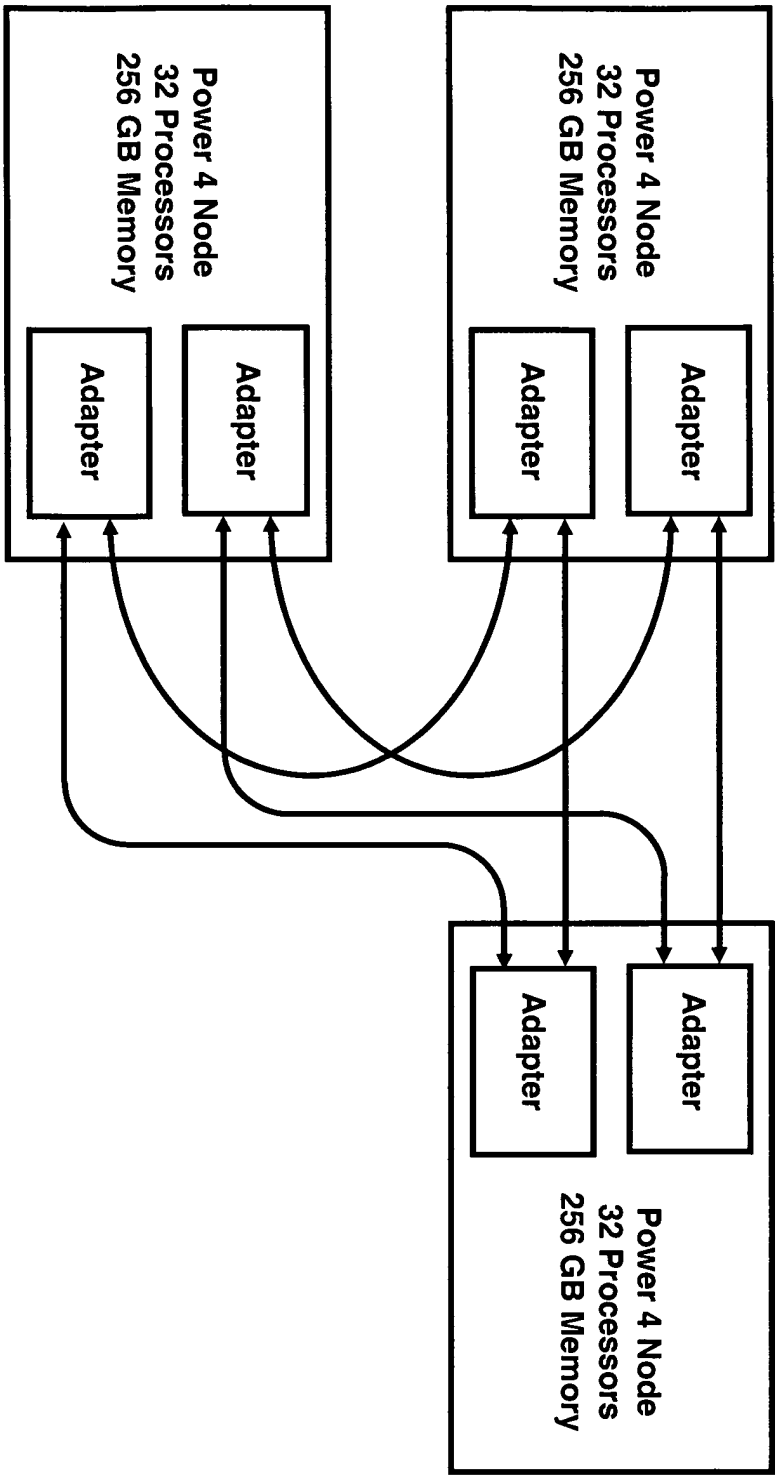
Power 4 Node
32 Processors
256 GB Memory
Adapter
Adapter
Power 4 Node
32 Processors
256 GB Memory
Adapter
Adapter
Power 4 Node
32 Processors
256 GB Memory
Adapter
Adapter

Figure 39

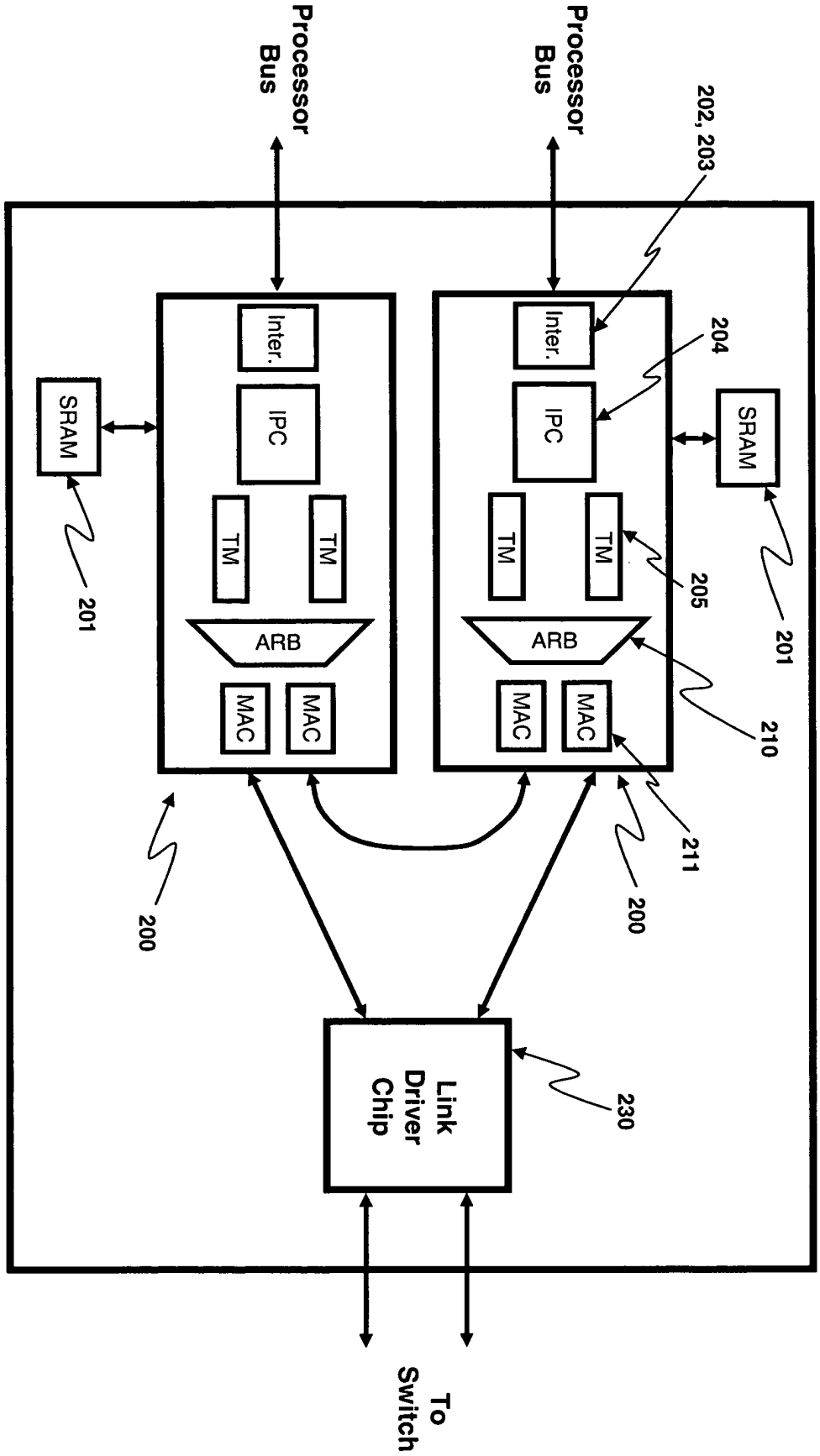
Processor Bus
Processor Bus
202, 203
Inter.
IPC
TM
TM
ARB
MAC
MAC
SRAM
204
205
201
210
211
200
200
201
Link Driver Chip
230
To Switch

Figure 40

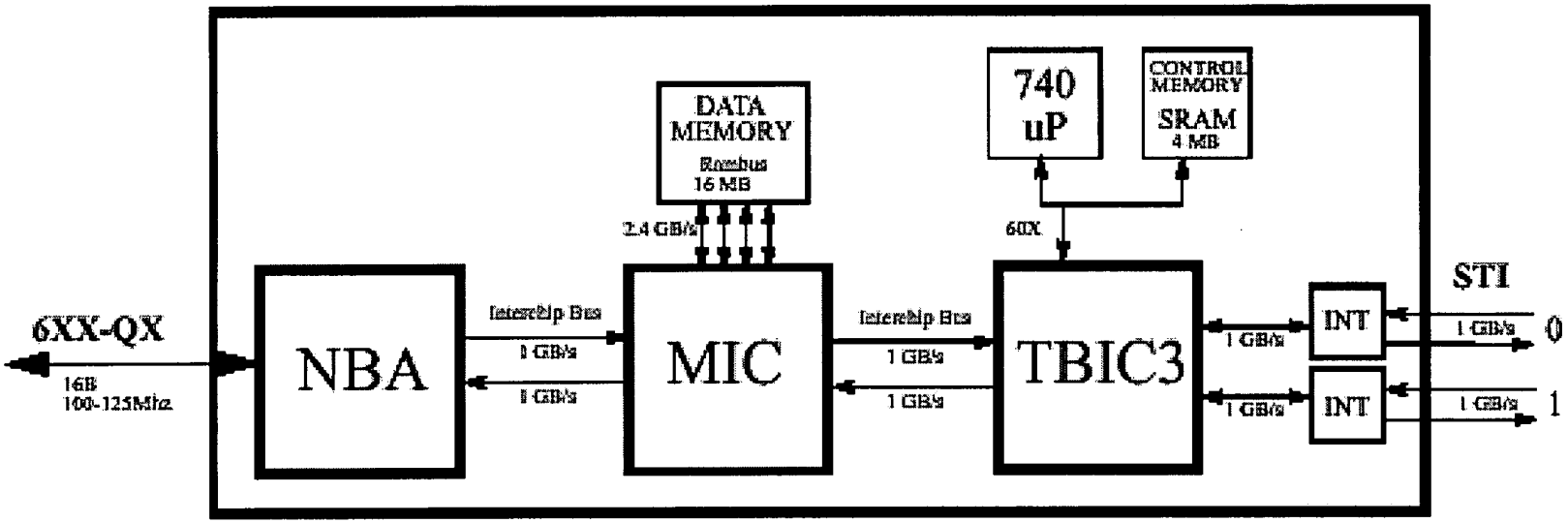

FIGURE 10. Colony Adapter

From page 32 of the spec – inclusion speculative

Figure 41

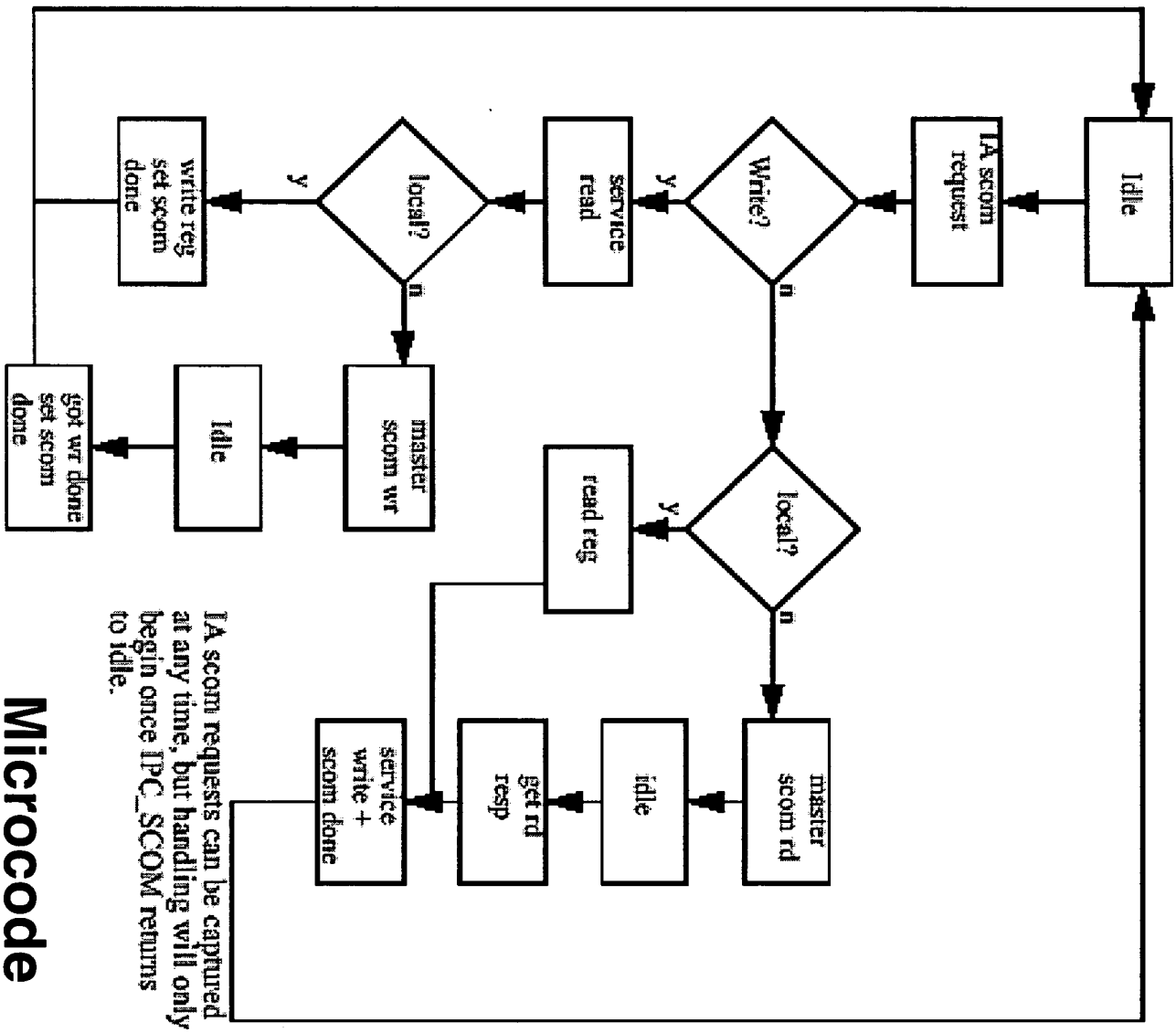

Figure 42 Microcode

AUTO TRACKING OF BAD PATHS

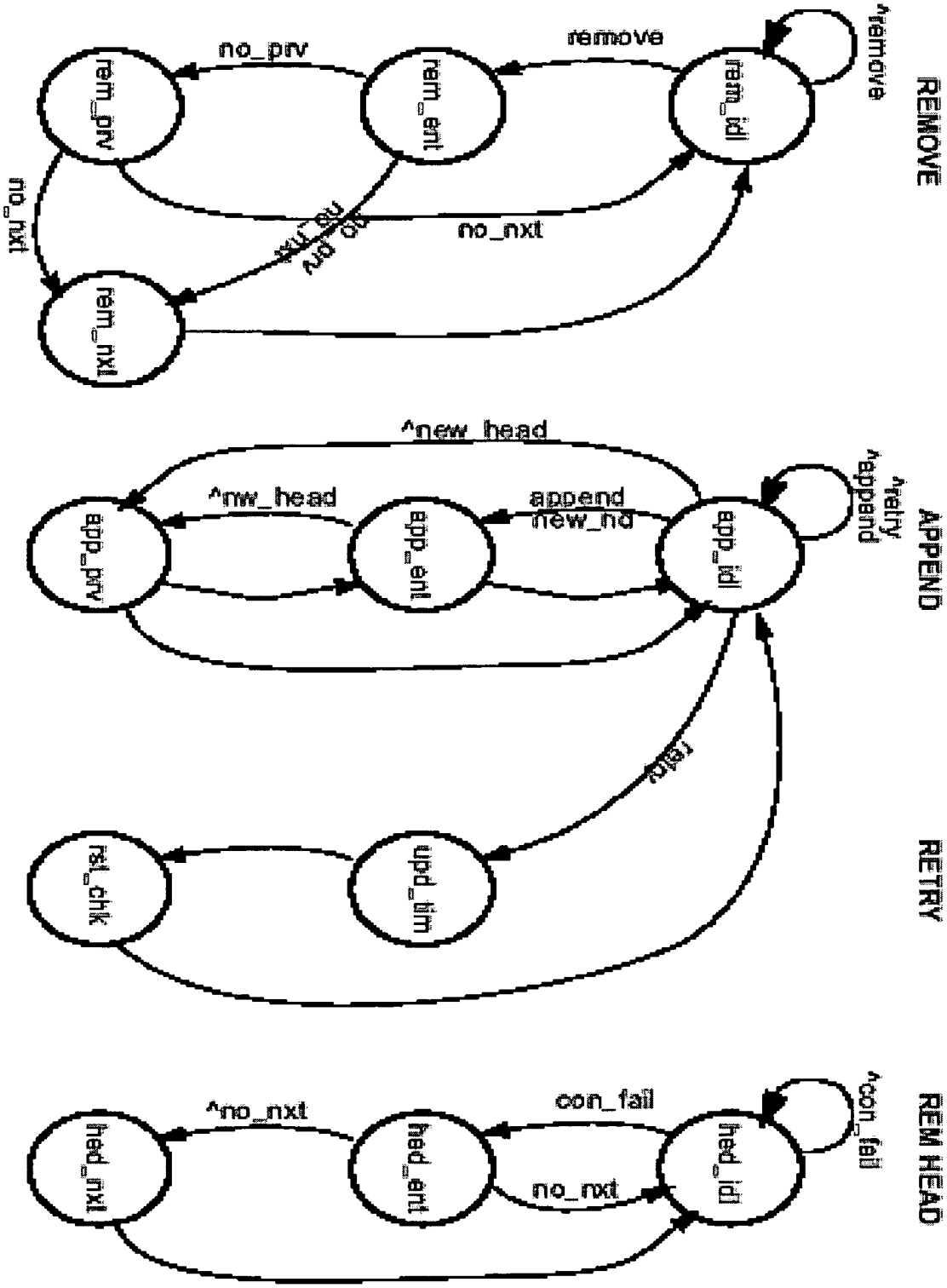

Figure 43

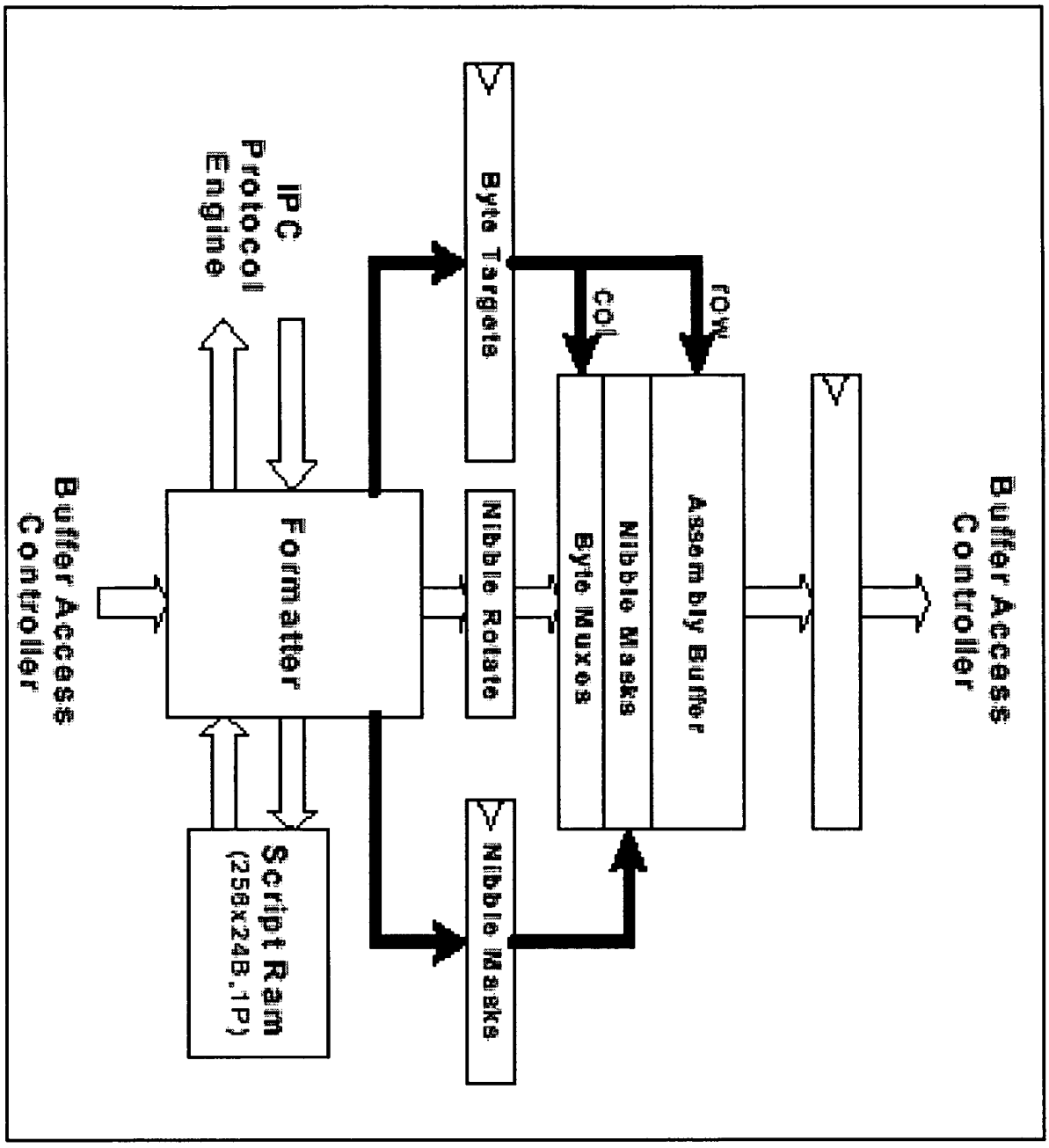
Formatter
Buffer Access Controller
IPC Protocol Engine
Byte Targets
ROW
COL
Assembly Buffer
Nibble Masks
Byte Muxes
Nibble Rotate
Formatter
Nibble Masks
Script Ram
(256x24B,1P)
Buffer Access Controller

Figure 44

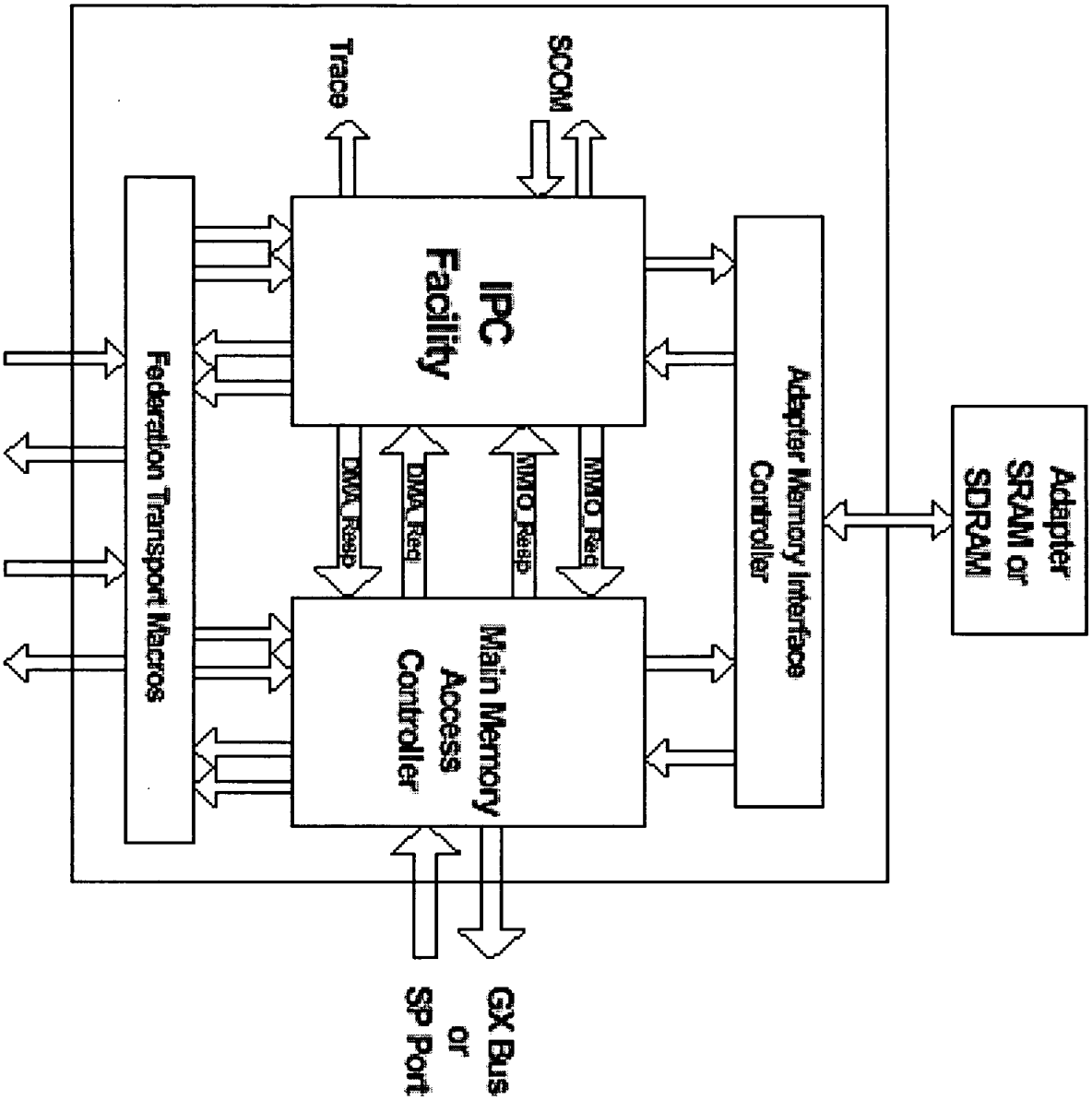
Adapter SRAM or SDRAM
Adapter Memory Interface Controller
Trace
SCOM
IPC Facility
Federation Transport Macros
DMA_Resp
DMA_Req
MMIO_Resp
MMIO_Req
Main Memory Access Controller
GX Bus or SP Port
Federation Fabric

Figure 45

Section 18

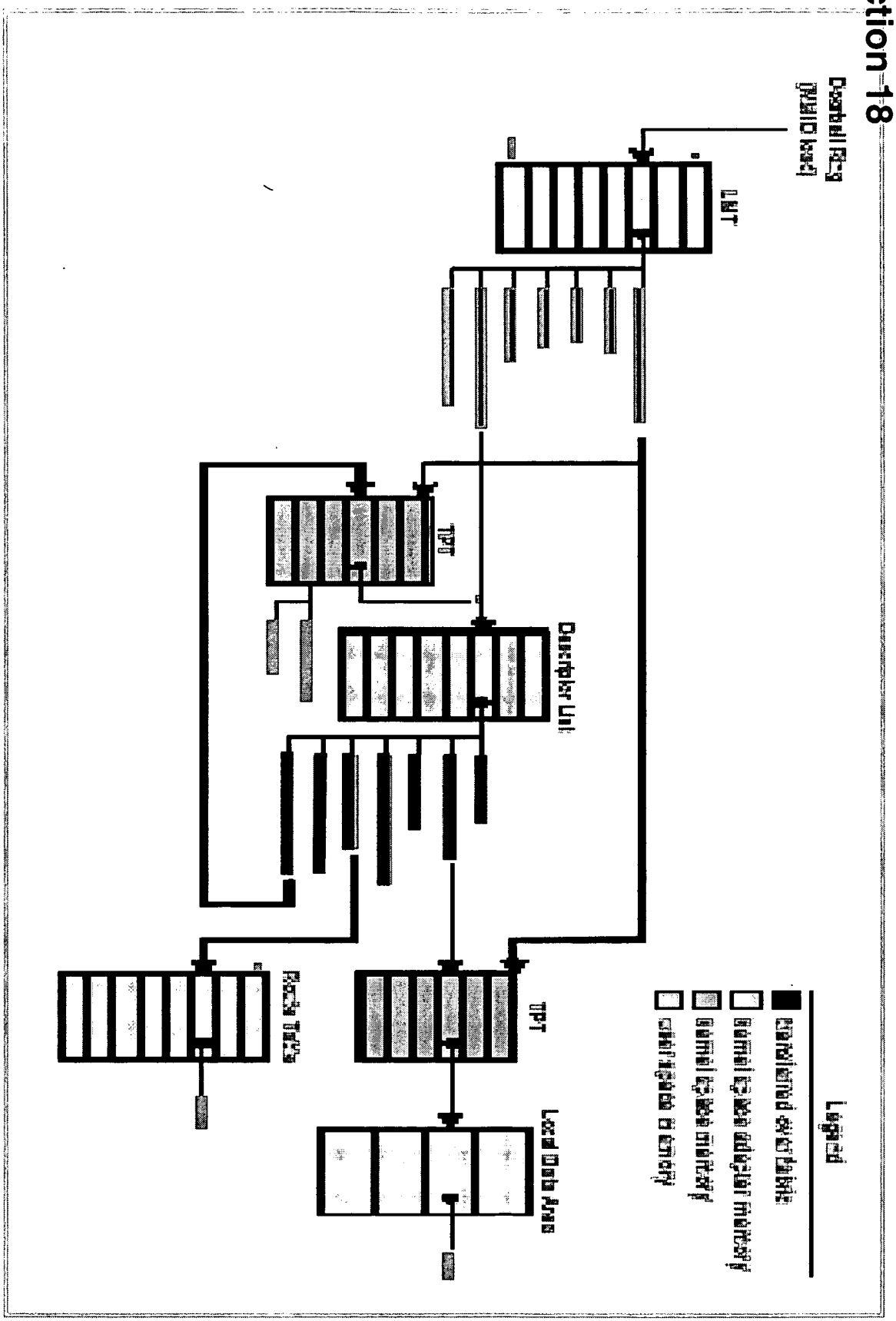

Figure 46

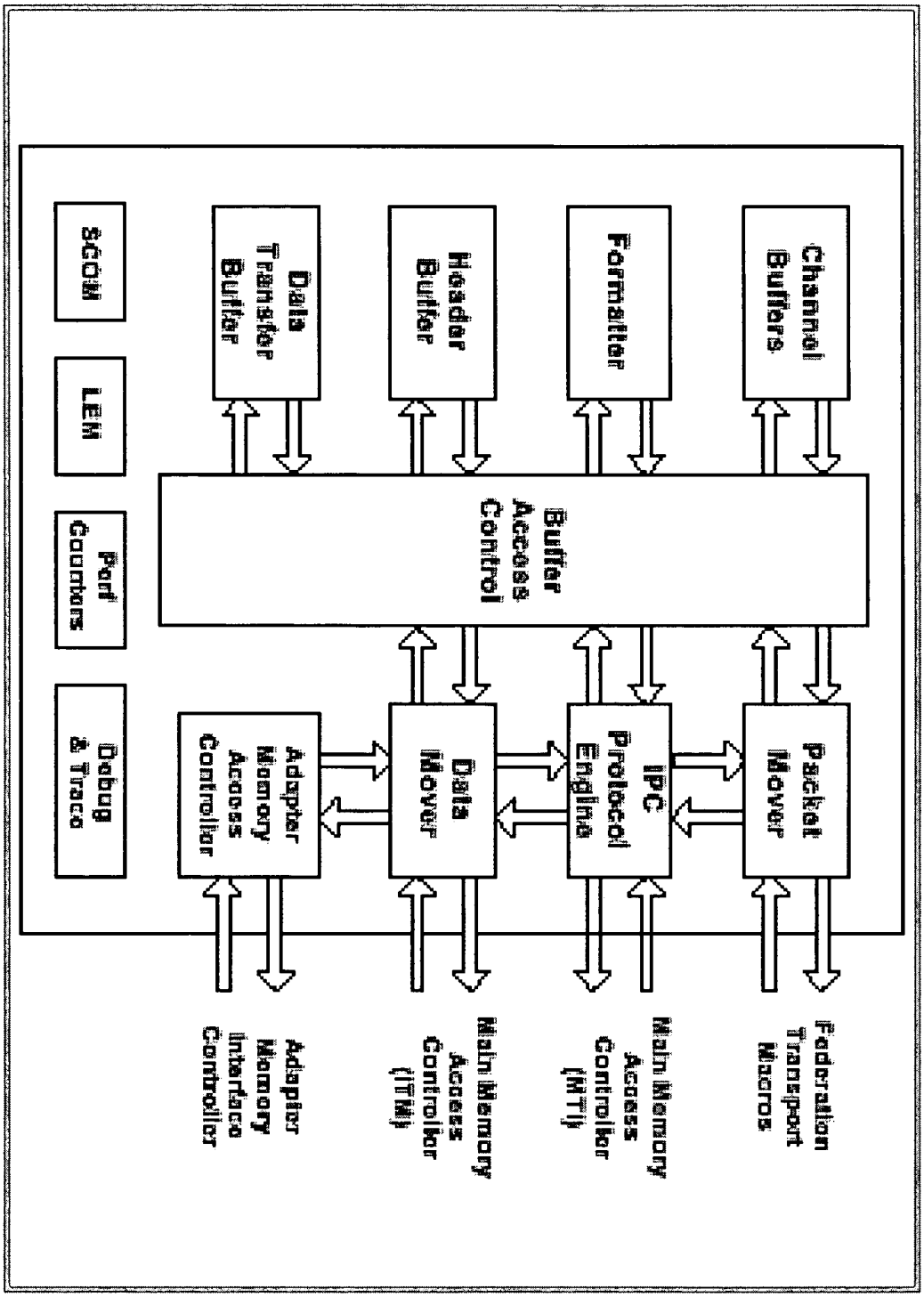
Channel Buffers
Formatter
Header Buffer
Data Transfer Buffer
Buffer Access Control
Packet Mover
IPC Protocol Engine
Data Mover
Adapter Memory Access Controller
Debug & Trace
Perf Counters
LEM
SCOM
Federation Transport Macros
Main Memory Access Controller (MTL)
Main Memory Access Controller (TTM)
Adapter Memory Interface Controller

Figure 47

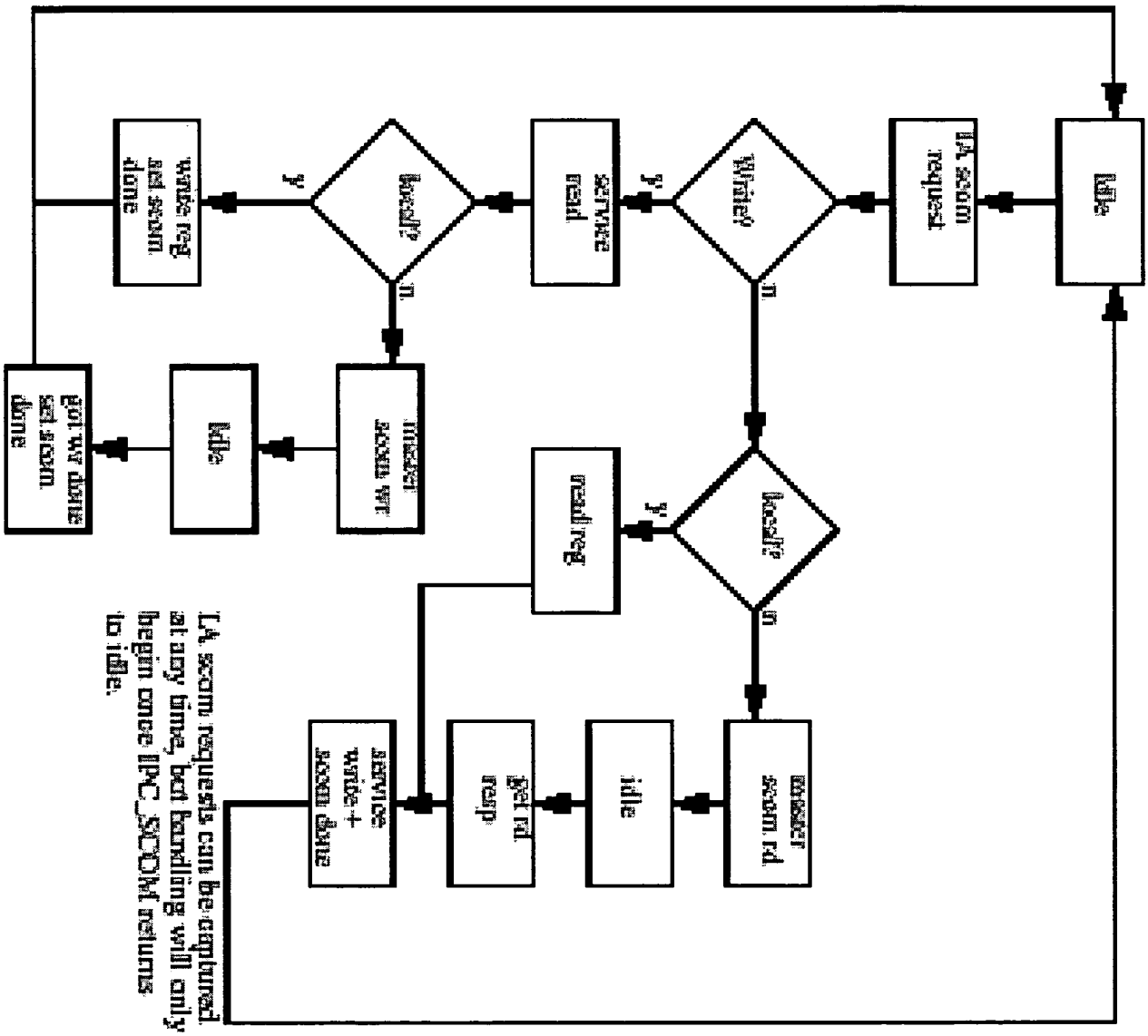
Idle
LA scom request
Write?
y
service read
hostIF?
y
write reg and scom done
n
master scom wr
Idle
get wr done and scom done
n
read reg
hostIF?
y
get rd resp
Idle
master scom rd
n
service write + scom done
LA scom requests can be captured at any time, but handling will only begin once IPC_SCOM returns to idle.

Figure 48

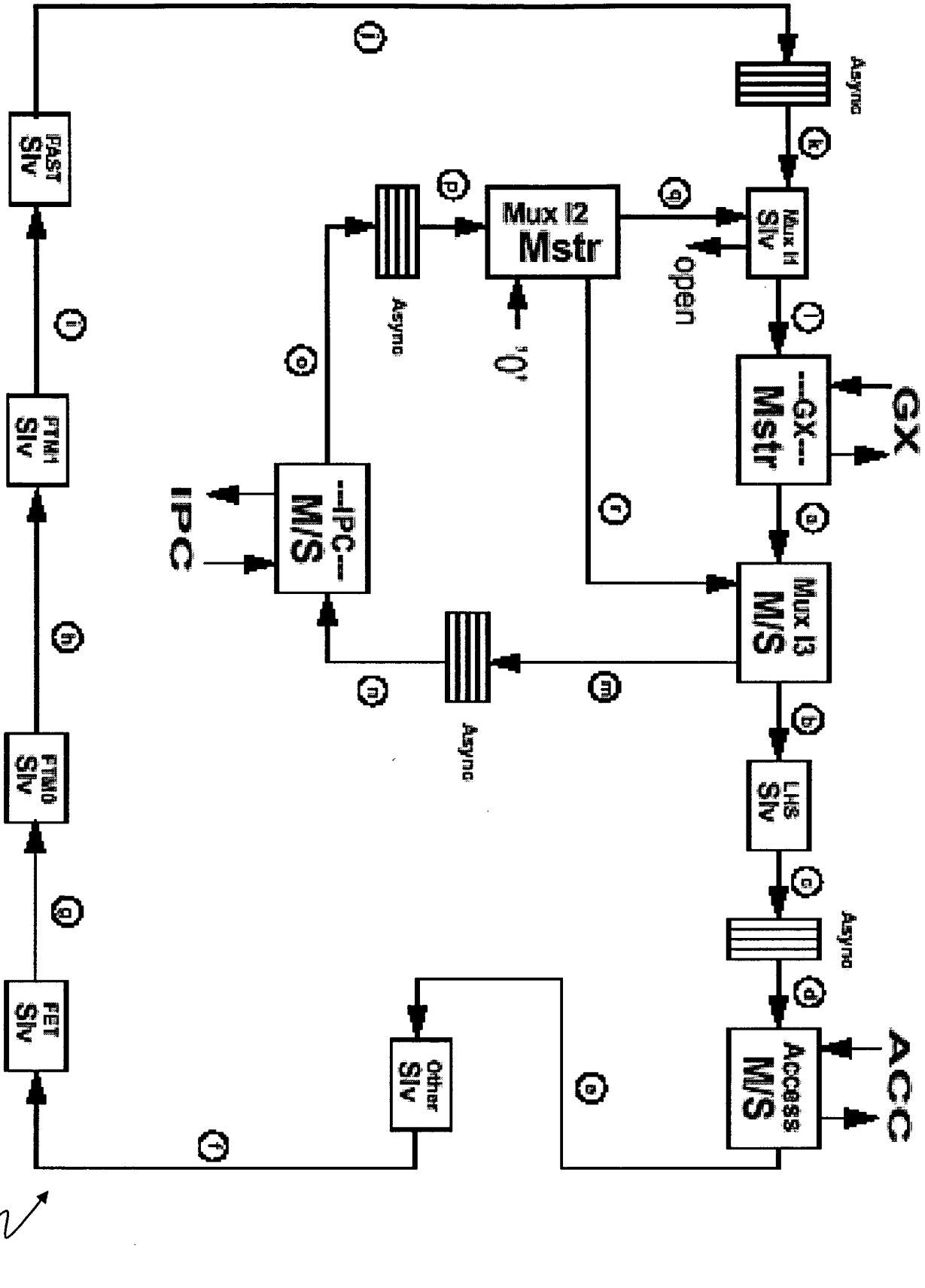
Async
Mux I1 Slv
Mux I2 Mstr
Async
'0'
open
GX Mstr
GX
IPC M/S
IPC
Mux I3 M/S
Async
LHS Slv
Async
Access M/S
ACC
Other Slv
FET Slv
FTM0 Slv
FTM1 Slv
FAST Slv
230

Figure 49

IPC Protocol Engine

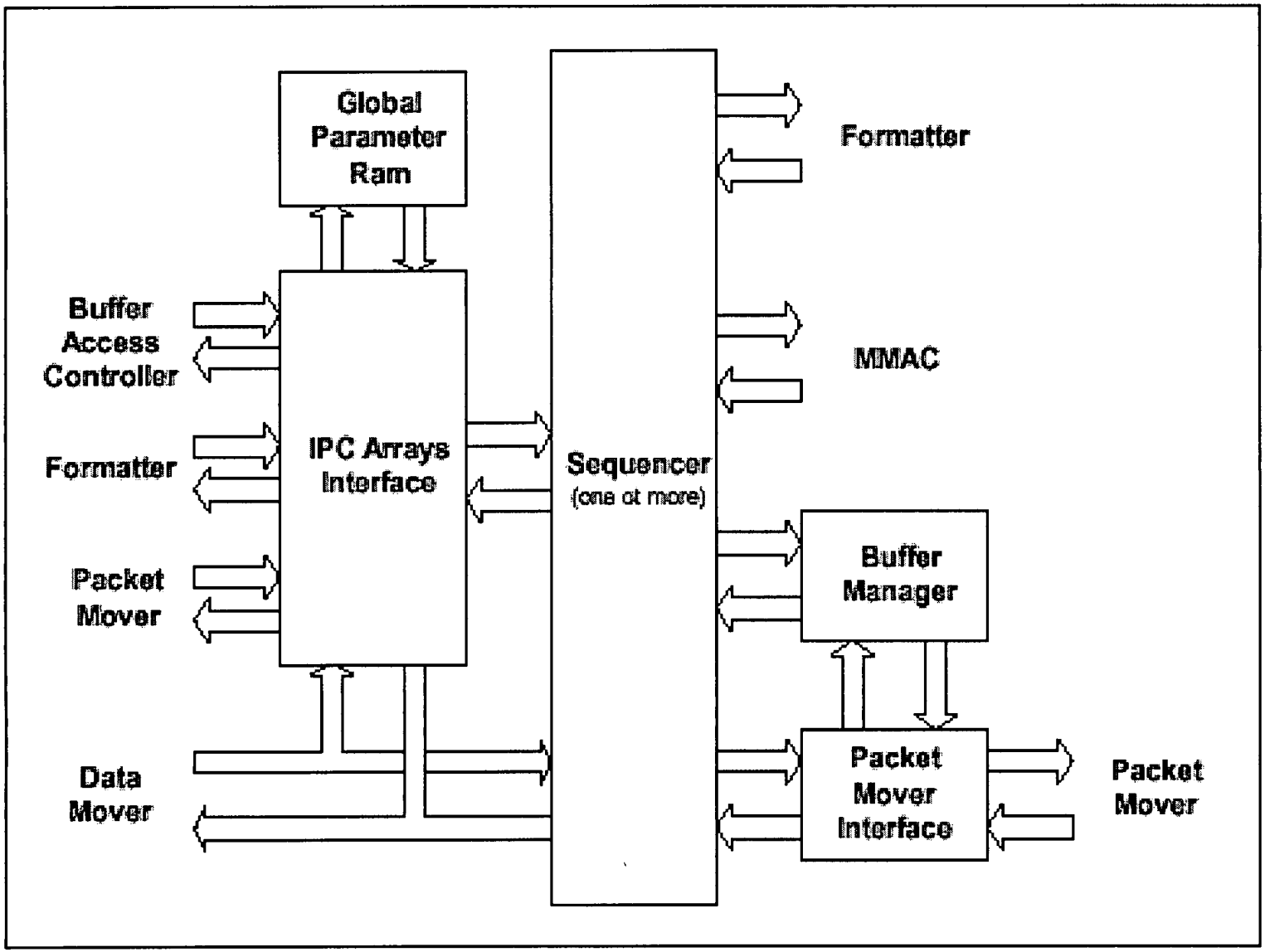

Figure 50